Module PCB product solutions

Contents

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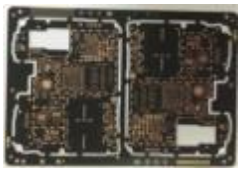
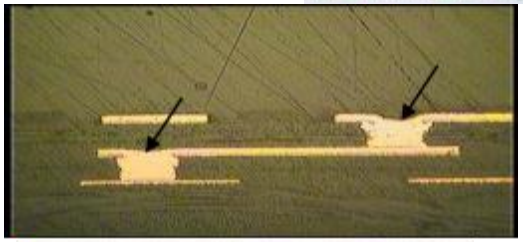
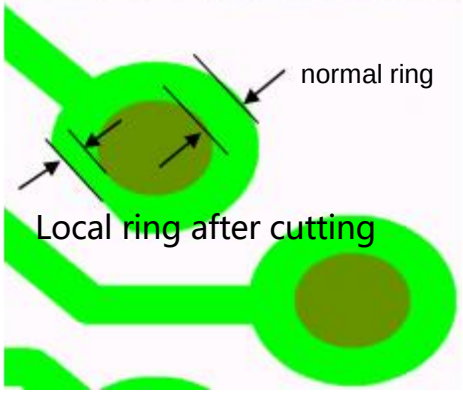
01 Product Process Capability

Communication terminal product design features and process capabilities:

Product design characteristics	Product technology capability
L/S	inner 45/45um outer 50/50um
Via	Min 3mil , aspect ratio < 1.0
Dimple	inner≤15um outer≤25um
PP	1027 (batch) 1017 (sample)
High alignment	Laser Ring cut Min2.1mil
application area	Mobile phones, tablets PC, e-books, etc





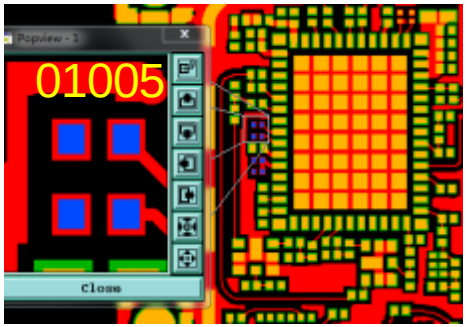


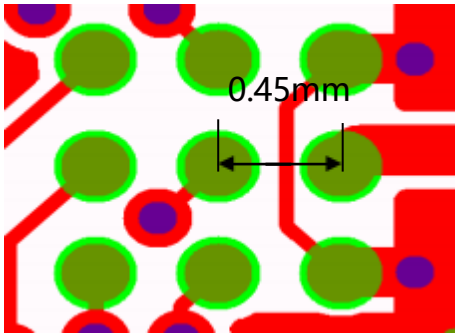
Consumer electronics product design features and process capabilities:

Product design characteristics	Product technology capability
High-order stacked holes	Order 6 HDI（12L ELIC）
POFV	Y
Line width tolerance	+/-10%
RF impedance	±8%
core plate Min	0.05mm
thickness of slab Min	0.55mm(8L ELIC）
application area	Smart wear, smart watch, smart Lock et al

Consumer electronics product design features and process capabilities:

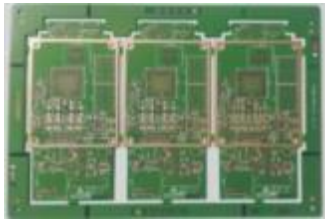
Product design characteristics	Product technology capability
BGA size Min	0.2mm
Minimum of BGA Pitch	0.35mm(no) 0.45mm(over 150 um wire)
BGA common difference	+/-10% or+/-30um
01005The welding pad	Y (0.16*0.14mm SMD)
application area	Drones, monitors, Bluetooth headset,Smart home appliances, etc

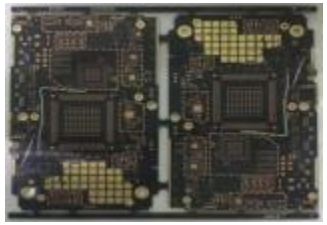


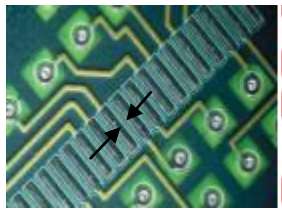
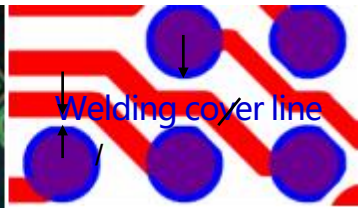


Communication terminal product design features and process capabilities:

Product design characteristics	Product technology capability
The thickness of the welding ink(Green / Blue / Black)	Line angle of 5 um Line face is 10 um
Minimum resistance welding Clearance	≥2.0mil
Minimum resistance welding Coverage	≥1.5mil
Minimum resistance welding bridge (green)	≥ 3mil
Minimum hole ring	4.5mil(3.5mil after cutting)
application area	Drones, smart speakers, monitors, and Smart door locks, etc

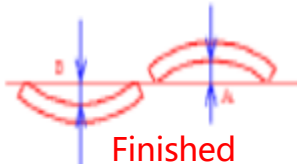





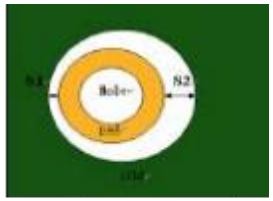




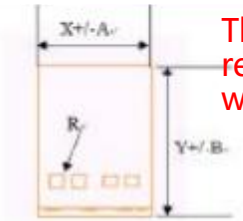
Communication terminal product design features and process capabilities:

Product technology capability	Product technology capability
Finished product warp (conventional)	≤0.5%
The accuracy of resistance welding	+/-1.2mil
Text-to-bit accuracy	+/-5mil
Forming size tolerance	+/-4mil
Graphics position tolerance	+/-2mil
Hole tolerance	+/-2mil
OSP to gold PAD distance Min	12mil
application area	Drones, smart speakers, monitors, smart door locks, smart home appliances, etc



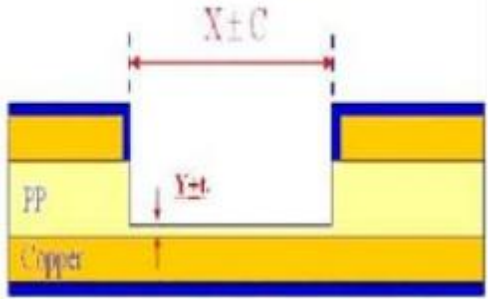
Finished warping





The accuracy of resistance welding

Forming tolerance



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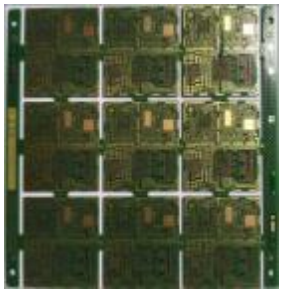
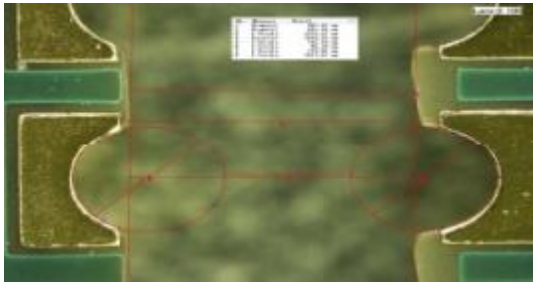
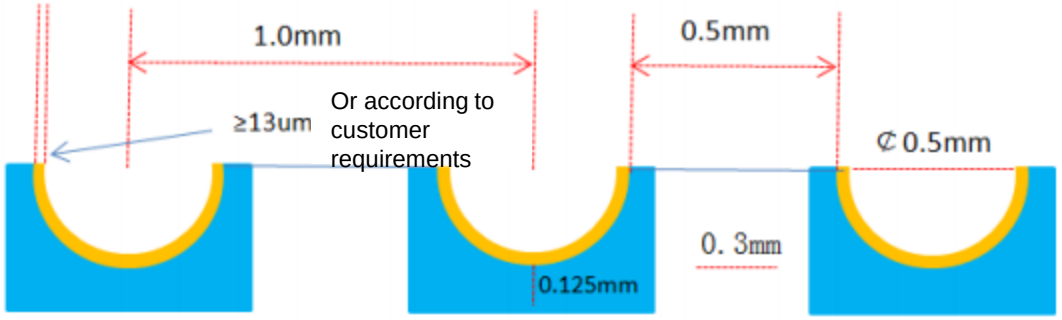
IoT module product design features and process capabilities:

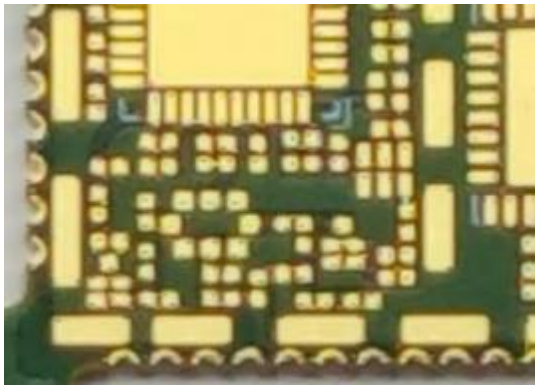
Product design characteristics	Product technology capability
Finished product warp Max	<0.5%
PTH half hole	Min ¢ 0.5mm
Half-hole Pitch	1.0mm
Minimum hole margin	0.5mm
Minimum copper PAD spacing	0.3mm
Minimum Tab bit width	2.0mm
The PTH half-hole fabrication method	Positive film pre-gong / negative negative gong
application area	Internet of Things expansion module

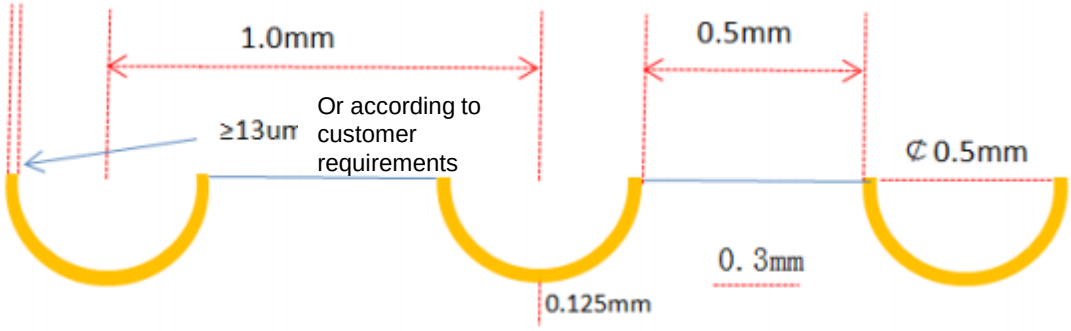


IoT module product design features and process capabilities:









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Industrial control product design features and process capabilities:

Product design characteristics	Product technology capability
Copper thick	Inner layer, Max 4 OZ Outer layer with Max 3 OZ + plating
Line width and line distance	0.10/0.10mm (per copper thick)
Kong copper	Regular 18 / 20 umSpecial requirements for plating of holes (e. g. hole copper 80 um)

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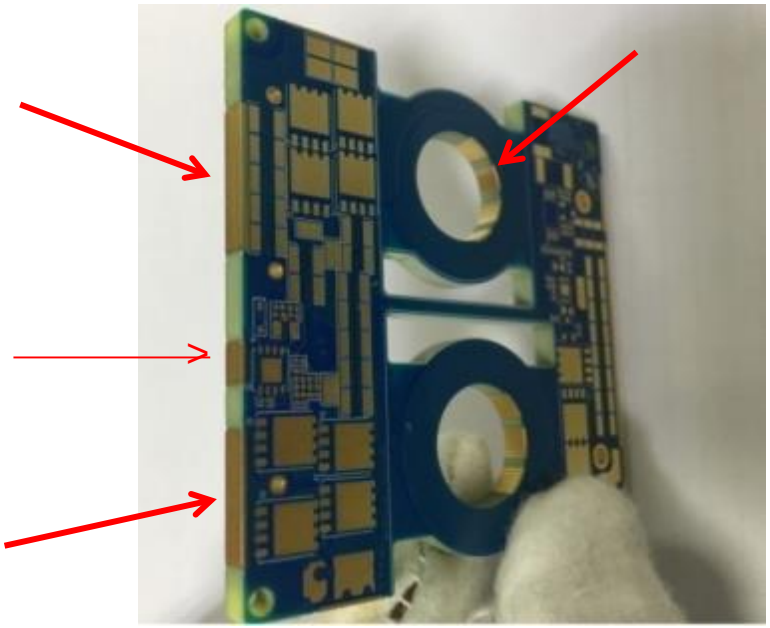
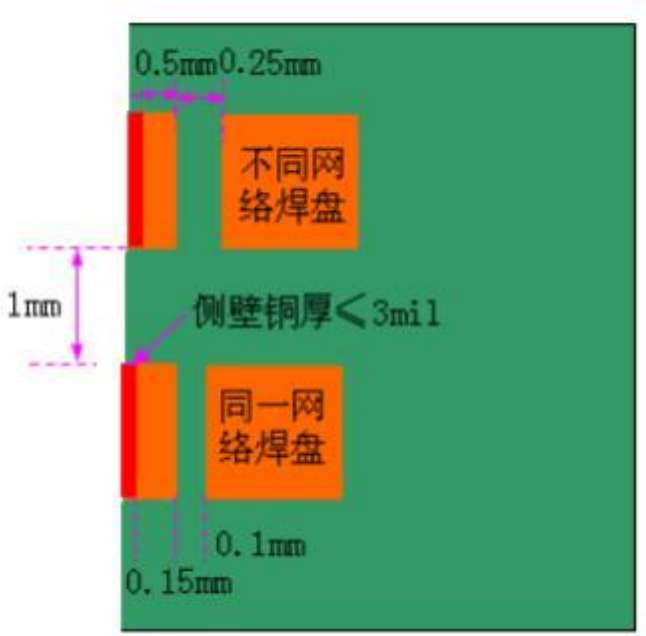
Industrial control product design features and process capabilities:

Product design characteristics	Product technology capability
Side wall electroplating	Width tolerance is ± 0.3 mm The pad flatness is ± 2 mil Side wall copper thick Max 75 um
Pressure resistance	Min1000V（≥50um） Min1500V（≥100um）
reliability test	Pressure withstand test, automatic inductance test, CAF resistance, Cold and hot circulation, hot oil, etc
application area	Power module

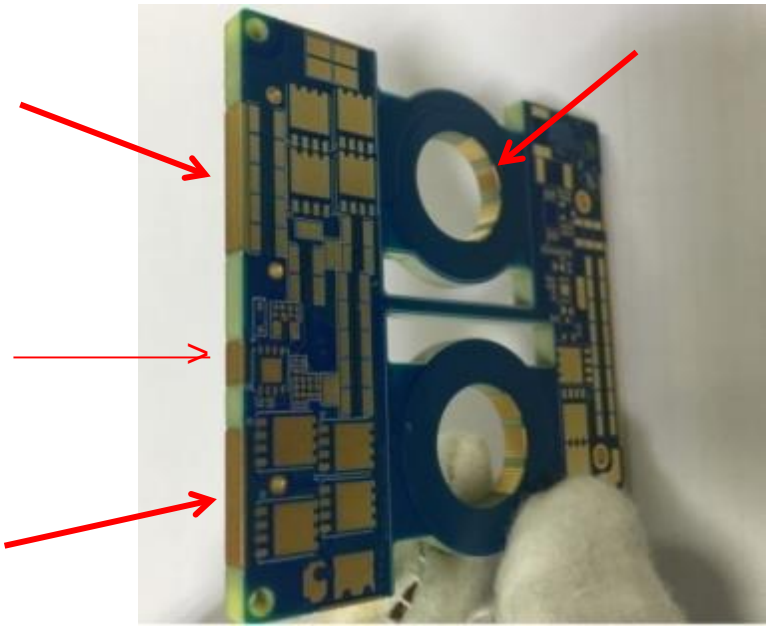
Industrial control product design features and process capabilities:

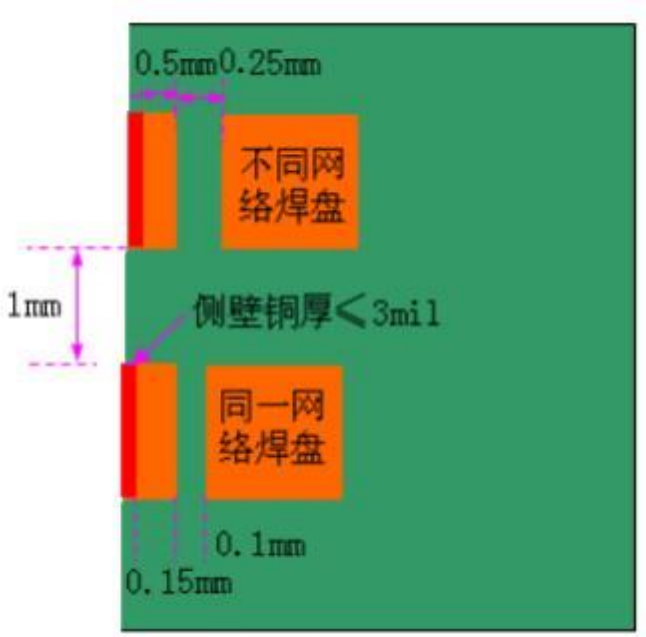




1. The side wall electroplating is made by the method of "pre-process-gong plate electroplating groove-copper plate electric- -outer dry film-graphic electroplating-pre-gong / pre-drill-SES —— outer AOI", which can ensure that the width tolerance of electroplating copper in the side wall is ± 0.3 mm, the flatness of the side wall welding pad is ± 2 ml, and the copper thickness of the side wall is controlled according to the conventional hole copper (the copper thickness of the side wall is currently Max 3 mil thick).

Industrial control product design features and process capabilities:



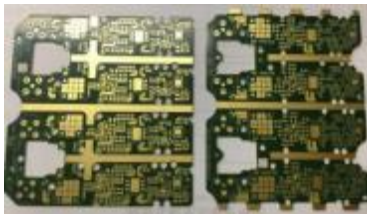


2. In terms of engineering design, it is recommended that the side wall electroplating spacing of different networks is 1 mm, the minimum width of the inner layers and the copper skin connecting the outer layer and the side wall is 0.5 mm, the spacing is 0.25 mm from different network pads, and the resistance bridge between adjacent pads.

Network communications product design features and process capabilities:

Product design characteristics	Product technology capability
High frequency high speed material	RO4730G3 / 4350B hydrocarbon high frequency material TC350 high thermal conductivity PTFE material M2 / M4 / M6 class high-speed material
High multi-layer	2~14L high multilayer with hole to copper Min 6 mil
Mixed pressure	High-frequency + FR 4 four-layer mixed-in pressure (RO4350B + IT 180A / S1000H, etc.)
Deepth control routing	Depth tolerance of ± 0.13 mm
coupling line	Winewidth tolerance ± 0.05 mm



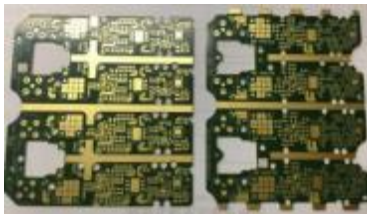






Network communications product design features and process capabilities:

Product design characteristics	Product technology capability
Back drill	Back drilling depth tolerance±0.1mm , Stub<10mil （ <2.0mm)
jumbo size	Max500*600mm
POFV	Pluhole hole depression <50 um and bulge <25 um
application area	AAU, BU, base station, power amplifier, antenna



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Data calculates product design features and process capabilities:

Product design characteristics	Product technology capability
High-speed material	M2 / M4 / M6 class high-speed material
High multi-layer	8~12L high multilayer,Hole to the copper in Min 6 mil
High vertical and horizontal ratio	Cros ratio Max12:1
Plug in damage	Purley / Whitley platform, Intel Detal-L method, 4 / 8 / 12.89 GHz
Skew control	5°, 10° line, trapezoidal convex block, thin cloth

Data calculates product design features and process capabilities:

Product design characteristics	Product technology capability
Back dril	Back drill depth tolerance±0.1mm , Stub<10mil （ <2.0mm)
Goldfinger	Ordinary golden fingers, long and short golden fingers
hypotenuse	Obevel depth tolerance ± 0.05 mm
application area	Server, memory bar, graphics card, photoelectric conversion

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Vehicle electronics product design features and process capabilities:

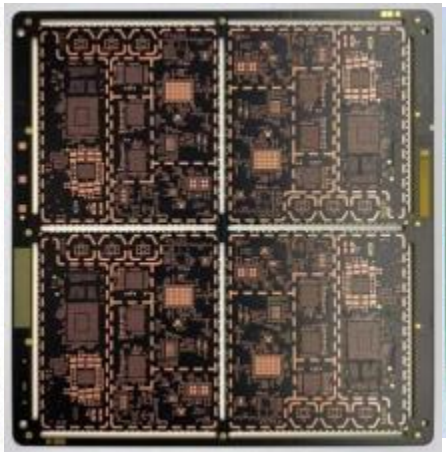
Product design characteristics	Product technology capability
material	FR 4, M2 / M4 / M6 high-speed material
High multi-layer	16L
thickness of slab	Max3.0mm
Back drill	Back drill depth tolerance ± 0.1 mm, Stub <10 mil (<2.0 mm)
Kong copper	18 / 20 um or IPC level 3 standard
reliability	CAF resistance (double 85 * 100V * 1000H),-40 to 120℃ cold and cold cycles 1000 Cycle et al
application area	Class B instrument, GPS, multimedia communication systemAnd all other Class C applications

02 Module PCB design characteristic

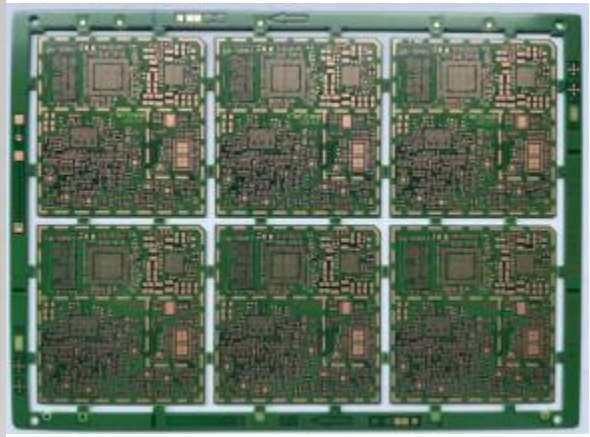
Module PCB product design features:

In communication, Internet of Things, automotive electronics, industrial control, military and other fields, more and more products modular design, such as radio frequency, Bluetooth, wifi, (2G, 3G, 4G, 5G) modules, positioning modules, etc. Module PCB products used on the plate, as a female plate, more through the metallized half hole and mother plate and components pin welding together, the whole row of metallized half aperture is small, the production difficulty is the half aperture control and hole ring design, RF impedance control, warping flatness control, module PCB also has a half hole design, its practice and ordinary PCB little difference.

Module PCB



PTH semi-hole module PCB



Non-PTH semi-hole module PCB

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Module PCB product design features:

In communication, Internet of Things, automotive electronics, industrial control, military and other fields, more and more products modular design, such as radio frequency, Bluetooth, wifi, (2G, 3G, 4G, 5G) modules, positioning modules, etc. Module PCB products are used for loading plates

On, as a mother plate, more through the metallized half hole and mother plate and components pin welding together, plate, the whole row of metallialized half aperture is small, the production difficulty lies in the half aperture control and hole ring design, RF impedance control, warping flatness control, etc., module PCB also has the half hole design, its difference with ordinary PCB.

PTH half hole

- Metallic half hole or one third of the hole, aperture is small, need to control the front and half, hole wall copper quality

Small size, thin board

- The module board Pcs is small in size, fine circuit, design, RF change, and sensitive, with high requirements on line width, intermediate thickness tolerance and uniformity.
- The module plate thickness is generally thin

High flatness requirements

- Welding disc flatness, high, part of the state strength requirements
- Finished product warping has high requirements

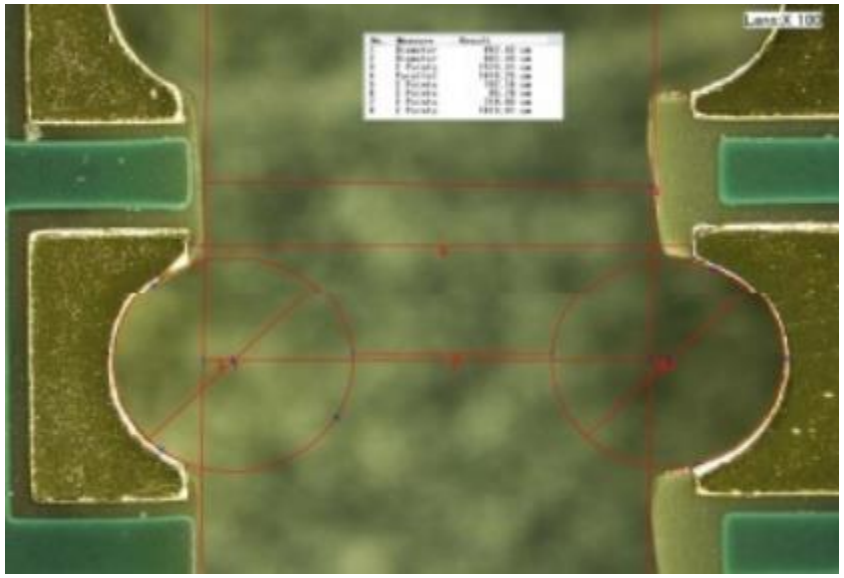
Strict appearance requirements

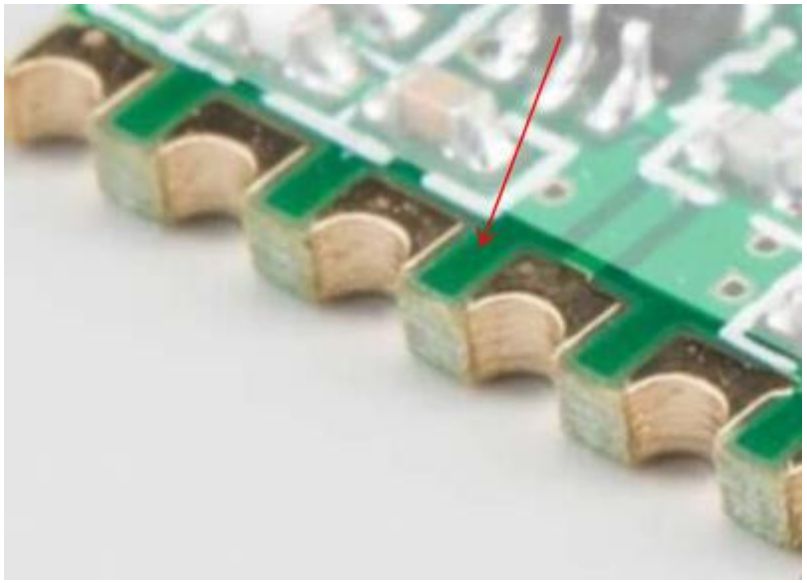
- Iot module board, after installation generally need to face, outward, the appearance requirements are relatively high

High reliability requirements

- High-order module folding, hole alignment, micro, blind hole processing, high reliability requirements
- High-order module products require multiple reflow thermal shocks and high reliability requirements for blind holes and boards.

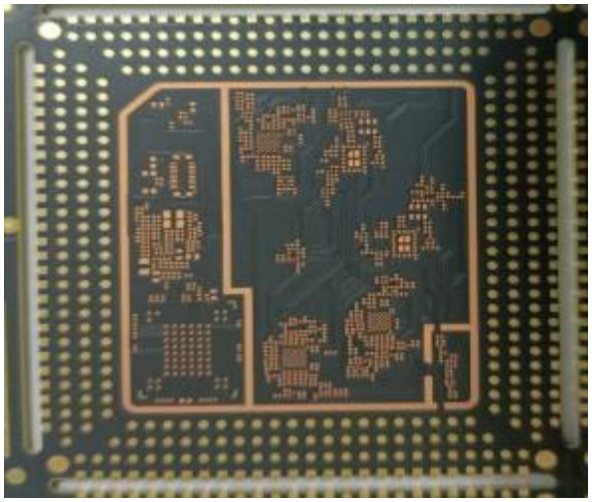
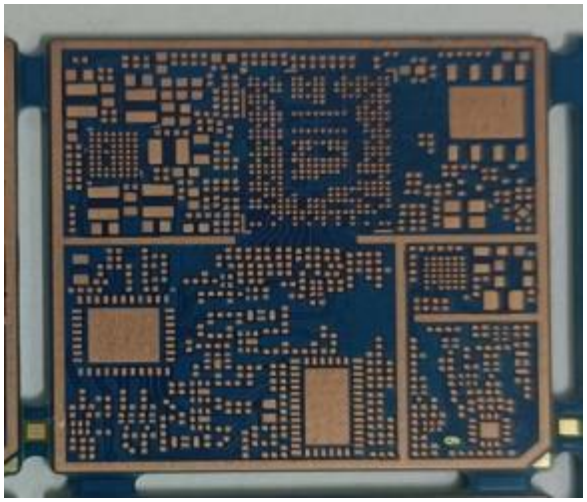
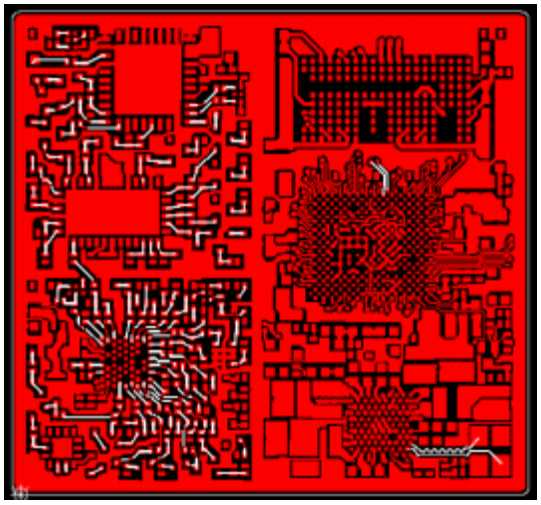
Module PCB product design features:





For the module products with PTH half-hole design, there are easy problems such as half-hole edge and half-hole copper deficiency in the processing process. Therefore, the control of PTH half-hole aperture, edge and half-hole effective area ratio (the industry generally requires half-hole ratio 135°, and individual items require 150°) control is a feature of module PCB. In addition, the position of the half-hole resistance welding window should be well separated from the character in the plate to avoid tin.

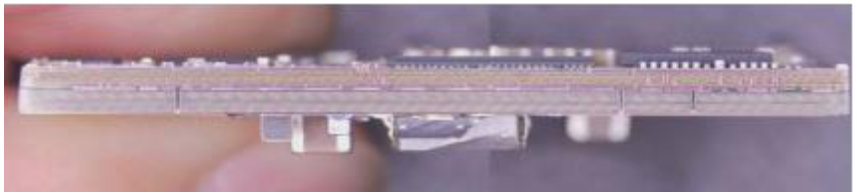
Module PCB product design features:

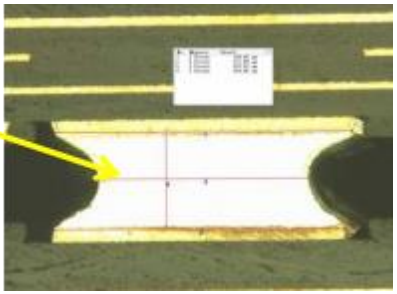




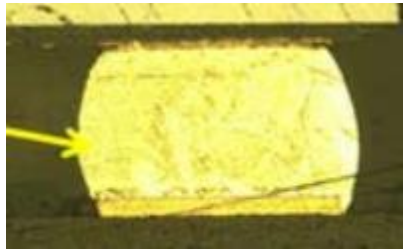
Module products are generally small Pcs in size and thin plate thickness, belonging to the typical "light, thin, short, small" design, and most of them are fine line design, and the impedance line width is relatively short, and the radio frequency changes are sensitive. In terms of design, the selection of overlapping structure,

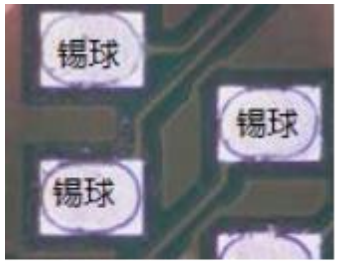
The line layout has high requirements. In PCB processing, due to the high requirements for impedance control, it also greatly increases the difficulty of controlling the line width, copper thickness and intermediate thickness during PCB processing.

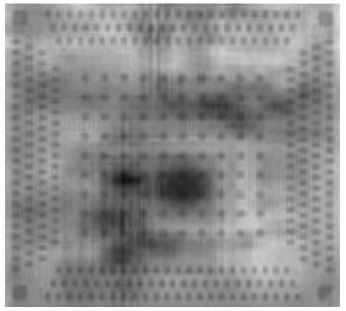
Module PCB product design features:









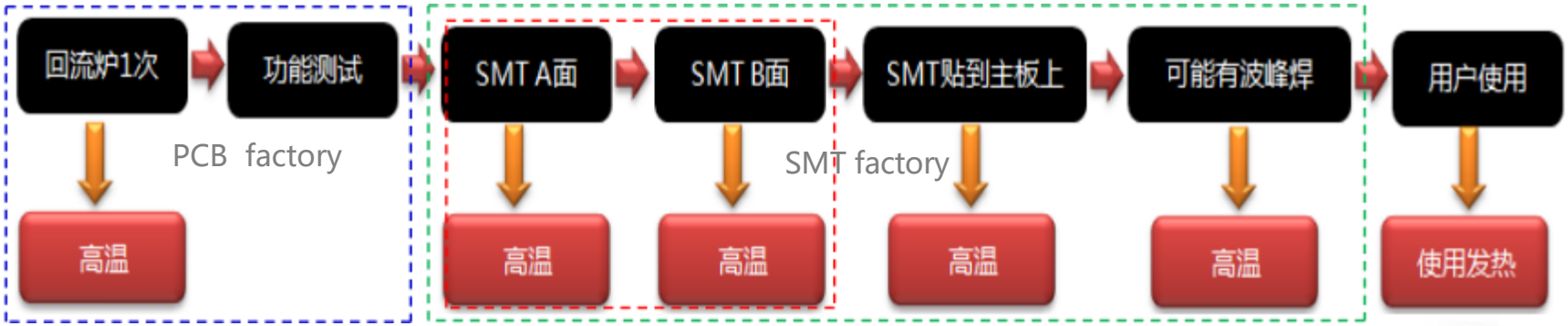


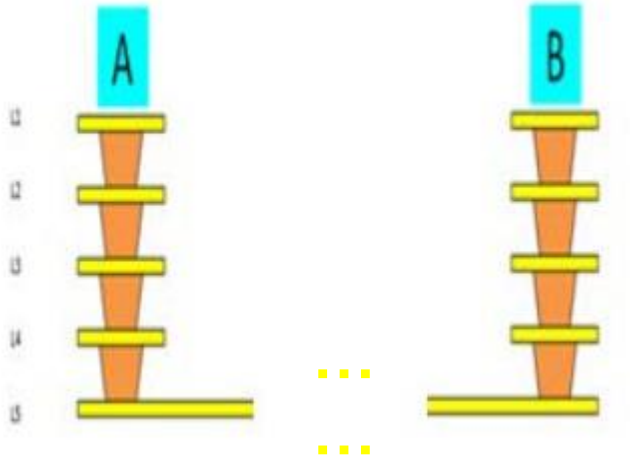
Module products need SMT to the main board PCB, most of which are single-sided SMT design (a few are double-sided SMT), most of which are shipped to the terminal in the form of PCBA. In addition to the strict appearance requirements, the board warping requirements are particularly strict, and the common PCB is generally

0.75%, the module board generally need to reach 0.5%, the more stringent need to reach 0.3%, the very individual need to reach 0.1%. When the warping of the module exceeds the standard, due to the small size of the welding pad, the small opening of the steel net and the small amount of tin, it is easy to lead to the virtual welding and the secondary folding, so there are special requirements for the stacking design, material selection, process processing and sticking process.

Module PCB product design features:

PCB heating analysis of higher-order HDI module:





1.1-2 order HDI because of only 1 layer or 2 layers of blind hole, when the heat impact, the heat is generally in the surface layer, with less impact on the internal PCB plate;

2. high-order HDI products, blind hole stacked hole into a copper column, blind hole copper column through L1-L4 layer, and the inner layer is connected through other lines, heat impact, heat conduction to the depths of the PCB plate, causing thermal expansion from the PCB plate, causing impact on the plate and hole chain;

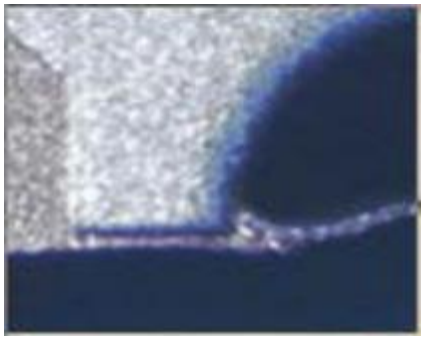
3. High-order module products need multiple reflux heat impact, which requires high reliability of blind holes and plates.

03 module PCB solution scheme

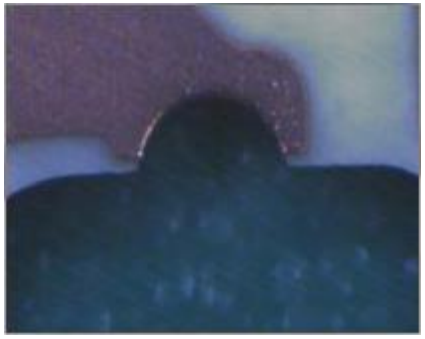
PTH semi-hole processing:

Before the process → drill → Gong PTH slot → Subin copper plate → Outer layer line → Graphic plating → Pre gong → Basic etching → After the process

Figure Pregong after plating tin



After the gong



The half-hole batch front was removed after alkaline etching

PTH half-hole module plate, with positive plate pregong, exposed edge, which can be removed after alkaline etching.

Plate processing scheme:

- sheet metal
  - Thin core plate processing
    - Device capacity is Min0.05 mm
      - Vacuum two-fluid
      - Horizontal submerged copper sink, VCP
  - Thin PP processing
    - No copper area spread copper bean / skin
    - Pressure range, typesetting mode, kraft paper, defined by the way to prevent the lack of glue, uniformity ± 10%
    - Classification of thin PP laser parameters
      - The Mitsubishi 5-generation machine, the DLD
      - DLD , 7-9um
  - Finished product warping control
    - The optimized residual copper rate at the design < 10%
    - Key process control
      - Open baking release stress
      - Pressure closing step cooling + step cold pressure cooling release stress
      - Weleld block tunnel furnace baking plate
  - Control of finished product fluctuation
    - The inner layer of film to rise and shrink pre-release
    - Process up and down drill belt, gong belt control
    - Automatic straightening machine, leveling and pressure baking





Thin board warping design optimization:

In order to improve the warping of the half hole plate, the outer side of the line and the other side is large copper skin, because the rate of copper residue on the two sides is different

Large, easy to produce plate due to uneven force, it is suggested: in the case of not affecting the electrical performance, consider the side of the large copper skin to a grid, reduce the difference of copper residue rate on the two sides, so as to improve the plate.

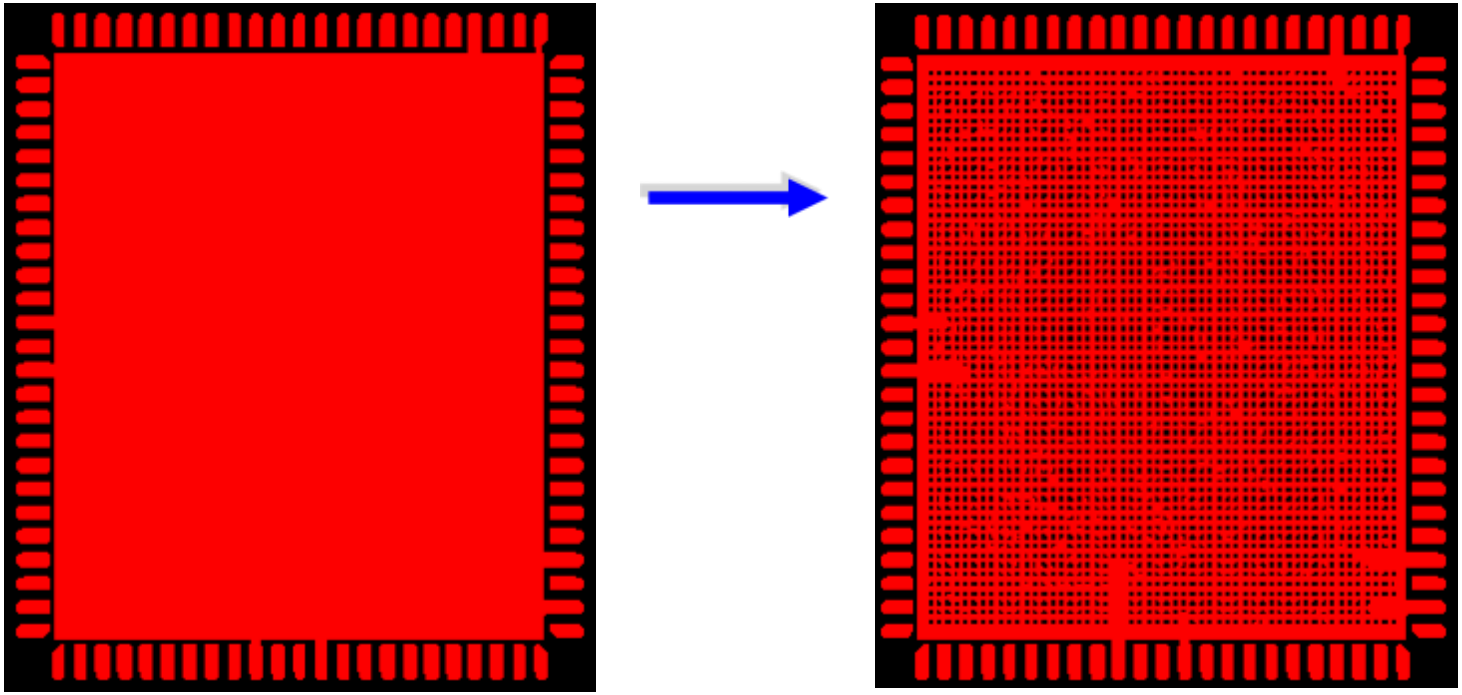


Plate warping, leveling and detection:

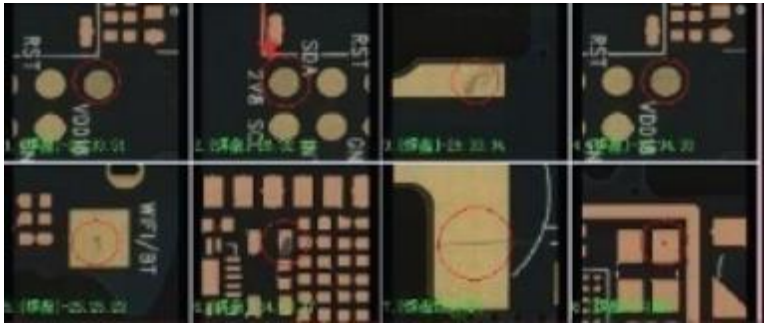
Flat the oven, leveling effect Max28%

Fully automatic warping machine——
The leveling degree is Max35%, and the change of fluctuation is within 1 / 10,000

Two confirmation of warping, automatic board warping inspection before shipment

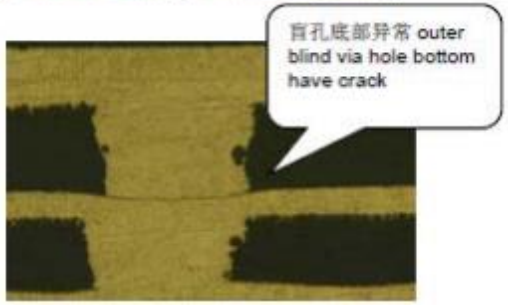
Visual AVI Inspection:

- Automatic appearance inspection machine:Image Yizhi 6, Shepherd 1
- Inspectable items:PAD, hole, word, oil, substrate, etc
- Production capacity: 1,900 square meters / day



Processing guarantee of microblind holes:

- Micro blind hole
  - design
    - Aperture design, 3.0-4.0m il
    - The aspect ratio is 0.6-0.8
      - Below the 1,080 PP
      - Cut the Pad after overall compensation
    - Laser, Ring>2.1m il
  - laser
    - Direct laser process
      - Brownalization, 7 – 9 um DLD
      - The Mitsubishi 5-generation machine, DLD
    - Laser parameters are subdivided according to PP and pore size
      - Laser energy and gun number optimization
  - Alignment degree
    - Burn target alignment, cross target alignment
    - Automatic rise and contraction, 2 mil interval rise and contraction
  - reliability
    - Laser aperture, + / -12.5um control
    - Laser / PTH / fill <48H / 6H
    - plasma / level removal /microablation
    - Process hot oil / HTC test
    - Two-and four-wire test after IR



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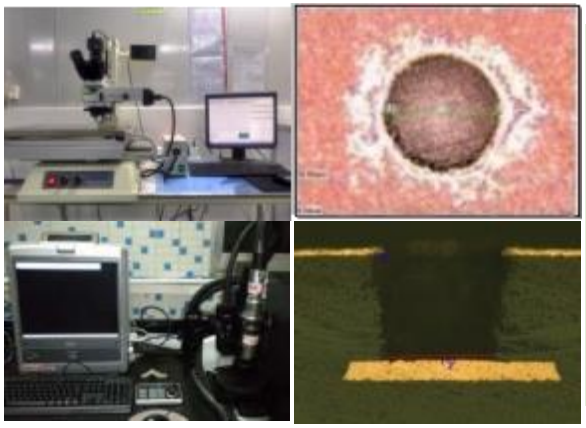
Processing guarantee of microblind holes:

Pore size: 0.075-0. 2 mm
Aperture tolerance: ± 12.7 um
Hole position accuracy: ± 25um

Mitsubishi I / / / V laser laser drill, 13

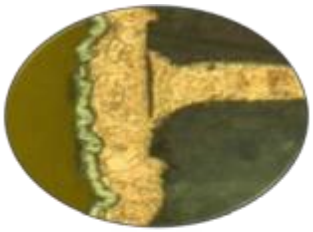
There are 20 large laser B / E / F laser drilling machines



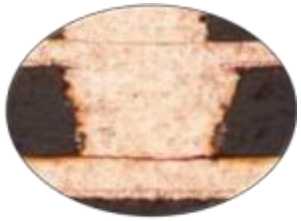
Monitoring of laser aperture and aperture type:
The OMT microscope
X500 X
Horizontal monitoring
Keens microscope
X 1,000 times the vertical monitoring

According to the average of 350,000 holes / Pnl, the theoretical capacity is 1900 square meters / day

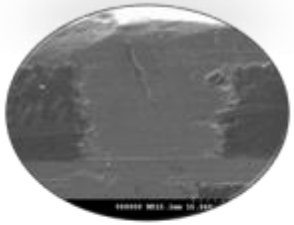
Baofeng Tang plasma processor etching uniformity> 85%, CF 4 / O 2 / N 2 / H 2 four-channel gas, suitable for FR 4, hydrocarbon high frequency, PPO high frequency, PTFE high-frequency, single-machine theoretical production capacity: 200 square meters / day



ICD NG

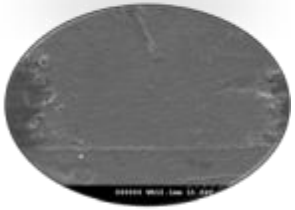


ICD NG



Blind hole bottom OK

(700X)



Blind hole bottom OK

(2000X)

Horizontal copper and VCP filling:

HDI special use Electroplating equipment

4 horizontal sunk copper wire:
The est plate thickness: 0.05mm
Single-machine production capacity: 1,000 square meters / day

1 # and 2 # cosmic spraying filling VCP line (moving frame), 3 # and 4 # cosmic soaking filling VCP line (fixed frame):
Dimple: Inner layer is 10um, 15um outer layer
Blind hole aspect ratio Max: 1:1, copper plating uniformity: ± 3 um single machine capacity: 2050 m 2 / day, plate thickness Min: 0.05mm

3#immersion type VCP

4#immersion type VCP

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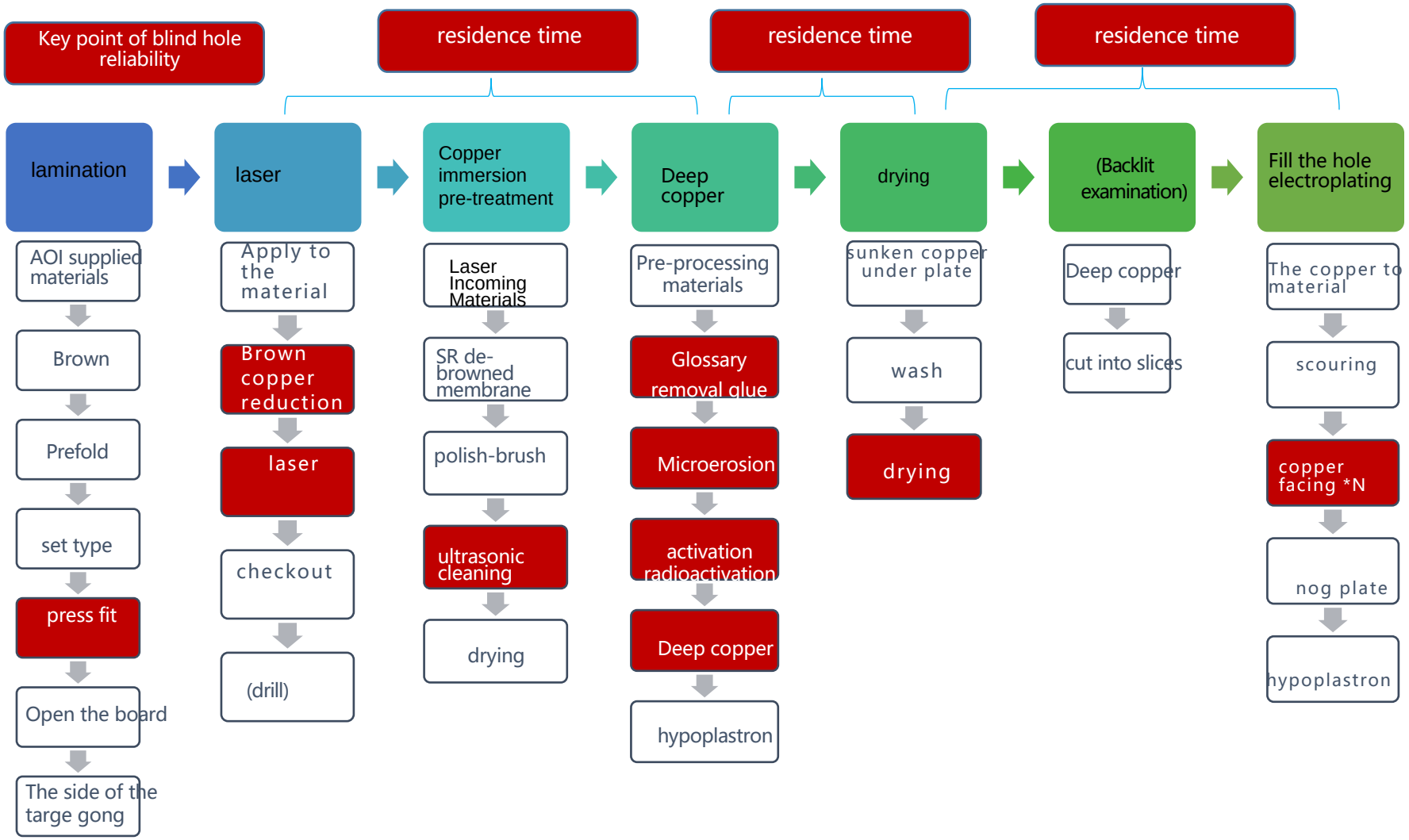
Identification of quality risk points:



"Press- -laser- -copper sinking- -filling plating" is the key manufacturing process of high-order HDI products. Blind hole bottom quality (bottom residual glue, bottom microcorrosion, bottom PAD oxidation degree) is the key risk point affecting the reliability of blind hole

Quality control of high-order HDI blind holes:

lamination

- High-order multiple compression process, material deformation affects the blind hole alignment, and the definition of material selection
- The accumulation of copper thickness uniformity affects the intermediate thickness uniformity, blind aperture, hole shape, and copper thickness uniformity control

laser

- Intermediate thickness uniformity affects the laser quality, aperture and pore type control
- Laser parameter control
- Partial accuracy control
- Stay time control after laser radiation

Deep copper

- Copper sedimentation before Plasma glue
- Micro-corrosion amount and ultrasonic strength control before copper settling
- Copper glue removal, micro corrosion control
- Drying effect and residence time control after settling copper
- Abnormal shutdown control

porefilling

- Residence time control from copper sinking to hole filling
- Environmental control of storage after copper sinking and before hole filling
- Pilling filling and parameter control
- Abnormal shutdown control

circuit

- Line alignment accuracy control





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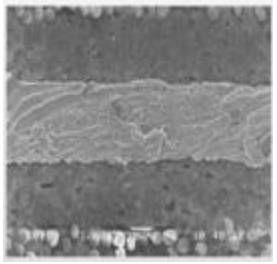
Reliability monitoring mechanism of high-order stacked blind hole:

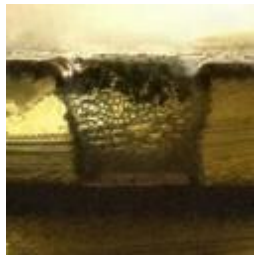
Hole diameter, hole type	Remove the amount of glue	Foreign body in the hole, blind, micro-erosion at the bottom of the hole	Rubber removal amount, micro-corrosion, amount, residence time	Residence time, hot oil, blind hole tension, HCT
laser	Plasma Remove the glue	Before copper sink treatment	Horizontal copper sink	Fill the hole electroplating

OMT microscope

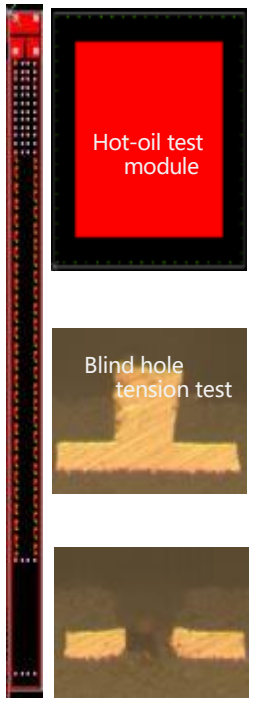


Plasma before glue removal

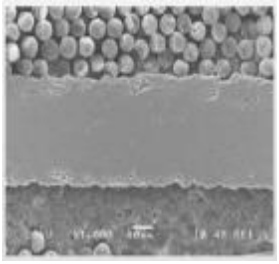
Copper sink front processing line



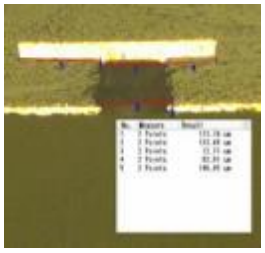
After blind hole removal



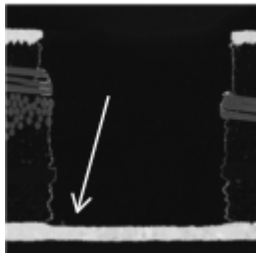
metallographic microscope



After plasma glue removal



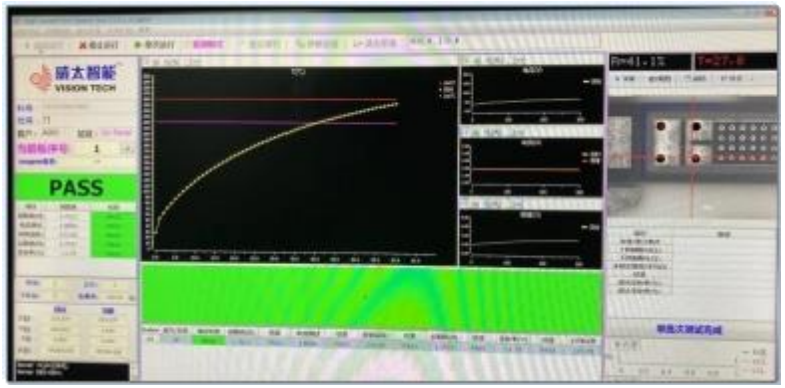
Ultrasound clear hole



Microerosion at the bottom of the blind hole

At present, there are different reliability monitoring mechanisms to monitor the thickness of the slice and Xray to the plating of semi-finished blind holes

Blind hole HCT and 2nd 4 wire tes
:



◆ HCT Coupon, 200 blind holes are designed on each surface, and HCT tests after the outer etch, which effectively monitors the plating integrity of the blind buried holes and the reliability of the bonding ability between electroplating copper

Four line test machine

Flying needle test machine

Automatic test machine

◆ Test accuracy of the four-line test machine:

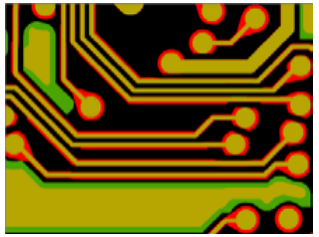
±1mΩ ±5%

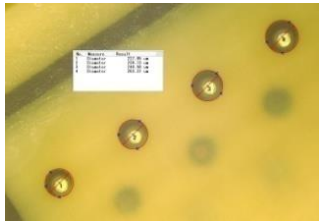
◆ Ultra V automatic test machine:

500-3000V (per customer requirements)

Fine line processing guarantee:

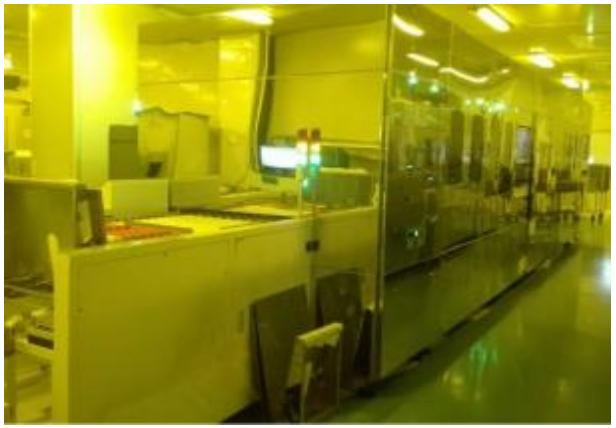
- Fine line
  - design
    - Line distance is Min40um, dynamic compensation, and line width consistency control
    - Set edge to add impedance bar, impedance consistency control, zero management
    - Process line width is strictly controlled, 5 / 9 point line width measurement / one side margin
    - Visual and test Coupon to monitor pad deviation
  - l a s e r
    - Laser cross target counterpoint, counterpoint accuracy ± 1.2 mil, line laser ring / compound target counterpoint
    - Automatic coefficient, 2 ml interval increase and contraction, improve the bias hole
  - electroplate
    - VCP plating, surface copper uniformity ± 3um
  - Transfig uration
    - 100% AOI scan, ship the AVI inspection pad
    - ORC LDI, Analysis of 30 / 30um, improve the film localization gap, pinhole
    - Figure transfer line / over-coarse resistance welding pretreatment to improve the collapse edge
    - Vacuum difluid etching factor> 4.0 and linewidth uniformity> 92%
      - Condai AOI 1.2 mil





LDI automatic exposure:

ADTEC LDI (3 sets in the secondary outer layer)
Parsing ability: 1.2 mil
Param accuracy: ± 0.7 mil
Single-machine production capacity: 1,200 square meters / day

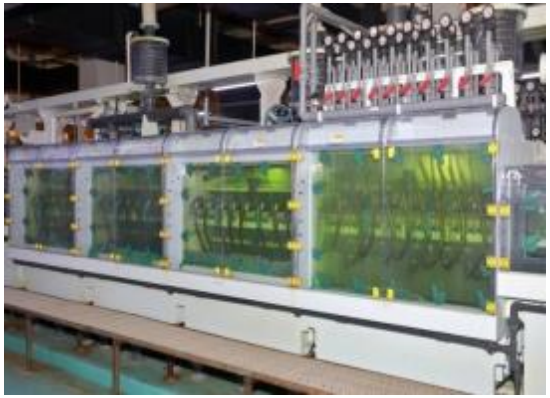


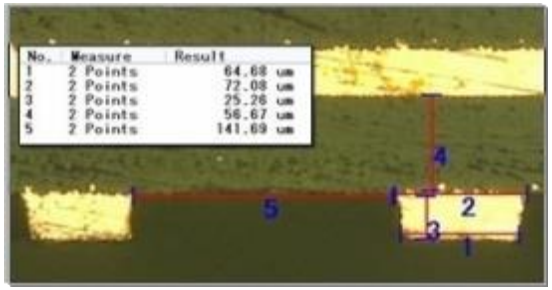
LDI (1 outer)
Parsing ability: 1.2 mil
Param accuracy: ± 1.0 mil
Single-machine production capacity: 400 square meters / day

Large Group LDI (1 outer line)
Parsing ability: 1.2 mil
Param accuracy: ± 0.8 mil
Single-machine production capacity: 550 square meters / day

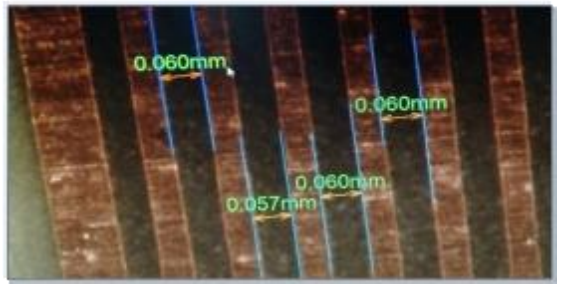
ORC LDI (1 secondary outer line)
Parsing ability: 1.2 mil
Param accuracy: ± 1.0 mil
Single-machine production capacity: 1,200 square meters / day

Vacuum difluid DES and CCD linewidth measuring meter:





Vacuum difluid DES etching effect: copper 25 um, margin 3.8 um, etching factor 7.0



Two cosmic vacuum difluid DES lines:

1. Automatic control of the pressure

2, with the etching uniformity of> 95%

3, the etching factor is> 4.0

4. Single-machine production capacity: 1,600 square meters / day

- Detectable items: PCB inner and outer layer after etching on the line, line, line width, spacing, hole and arc diameter, etc
- Features: precision focus, automatic edge seeking, sub-pixel algorithm
- accuracy:+/-1um

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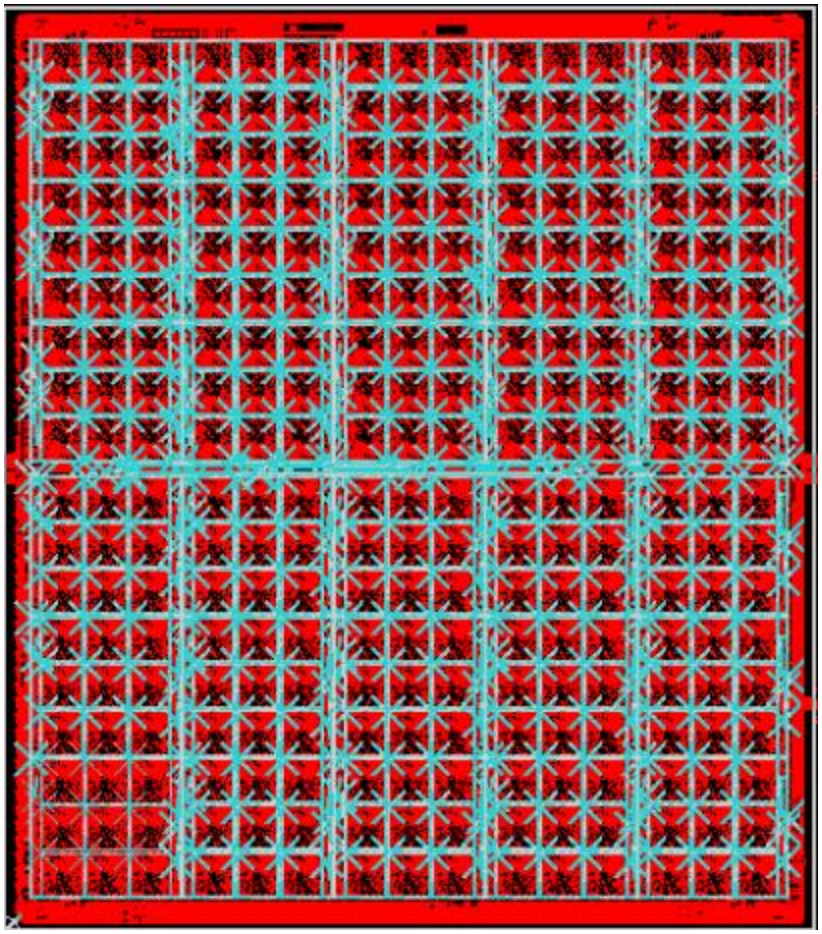
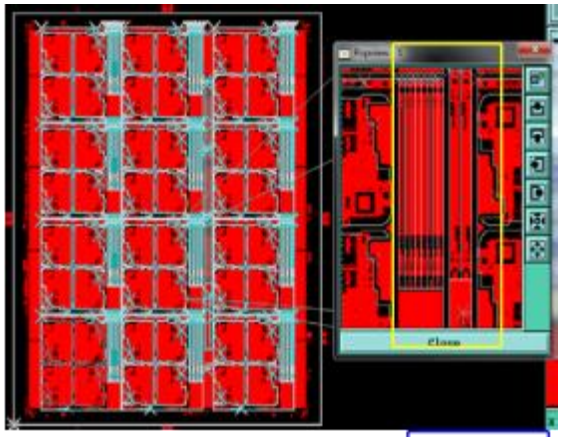
Module PCB Impedance Return to Zero Management:

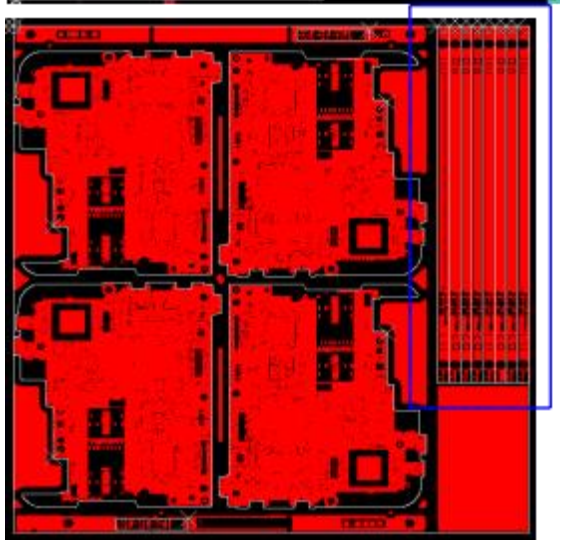
When the module board is WPNL, the module board keeps the edge according to the product structure, and the edge of the module board is> 20 mm. The intermediate thickness difference caused by the flow glue of the plate is reduced by increasing the edge, so as to ensure the consistency of the flow glue during pressing and avoid the influence of the intermediate thickness difference on the RF impedance.

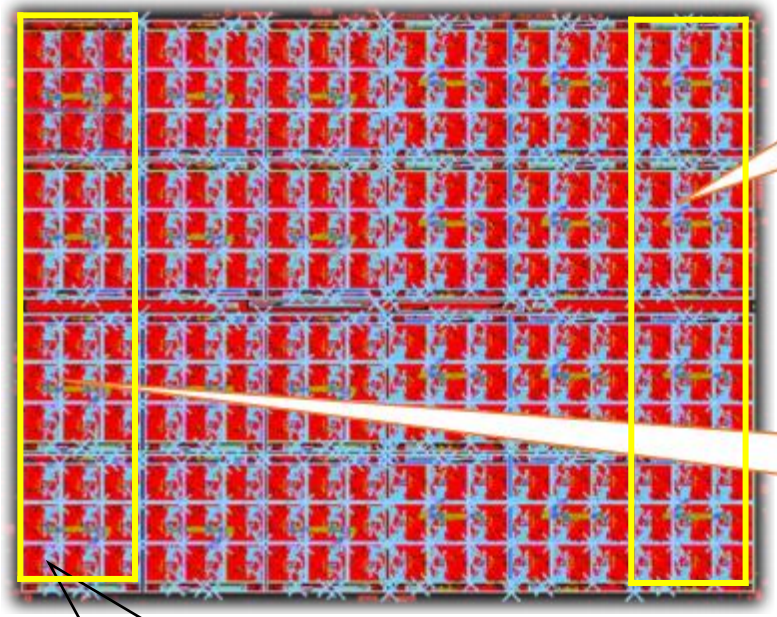


Module PCB Impedance Return to Zero Management:

On the WPnl panel, single end impedance strip is added for each Set to monitor the Coupon line width and impedance value during the process to ensure that the difference between the internal impedance and Coupon is within the range of 2 ohm.

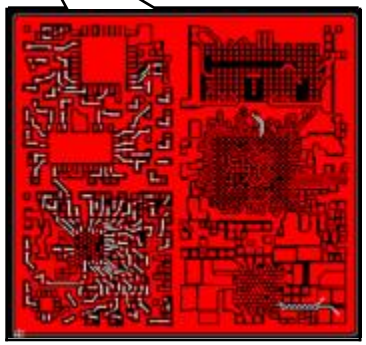






This part of impedance, line all left (inside)

This part of impedance, line all to the right (inside the plate)



In the Set in the working block WPNL, the white radio frequency line is designed to avoid being close to the adhesive edge and reduce the impedance affected by the uneven medium layer and line width of the plate edge.

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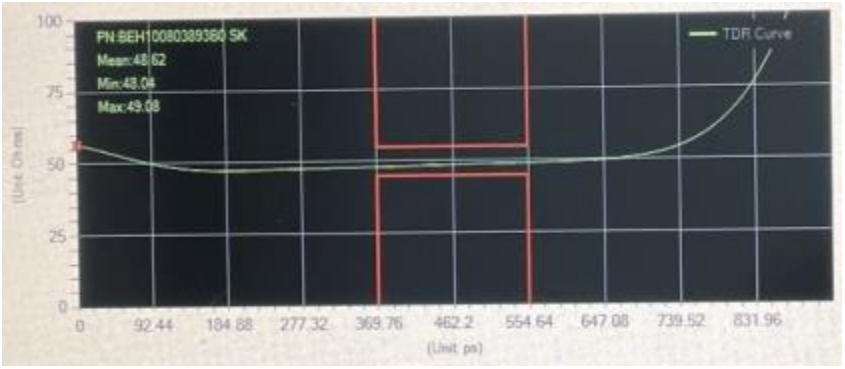
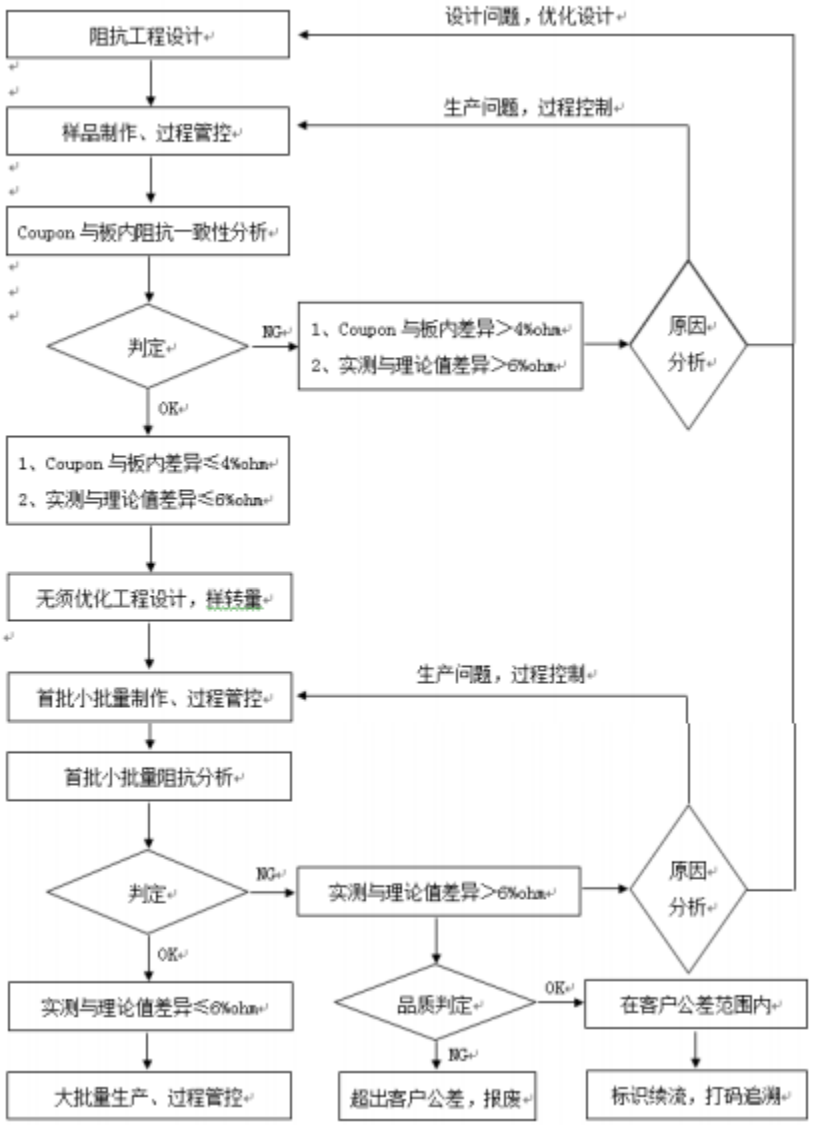
Module PCB Impedance Return to Zero Management:

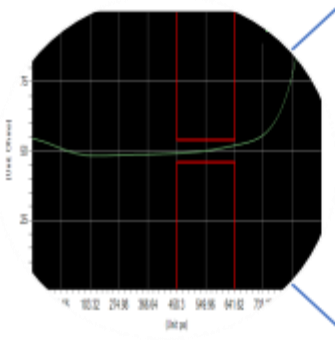
1. In the sample stage, the impedance is consistent between unit, Coupon and design:
① The measured / simulated Coupon impedance value shall be 4% ohm different from the unit;
② 6% ohm;

2. In the first stage of small batch, the impedance is measured and theoretical value consistency analysis:
① The measured / simulated Coupon impedance value and the design median difference are 6% ohm





Module PCB Impedance Return to Zero Management:



Line width zero

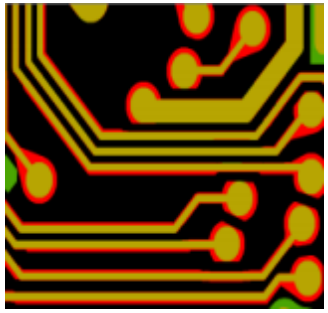
- Work draft dynamic compensation
- 9-point normal width uniformity analysis

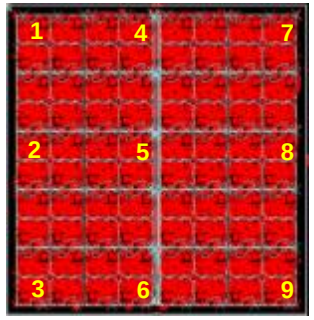
Mediate thick return zero

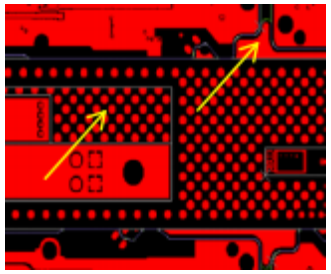
- PNL copper paving optimization
- Fixed compression and closing parameters
- Fixed typesetting mode

Copper thick return zero

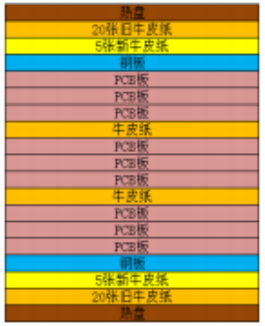
- Fixed process flow
- Fixed production line body
- Fixed process parameters





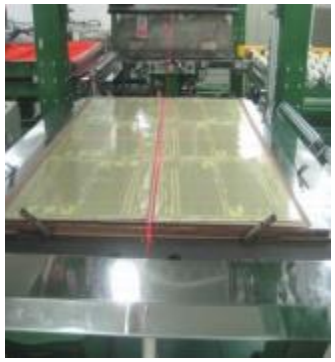


压合程式：M6，排板层数：10层，中间垫两次牛皮纸、上下使用各25张全新牛皮纸。



1. When designing engineering impedance, the median value of impedance design shall be within + / -1 ohm required by customer specifications;
2. In the production process, the line width, intermediate thickness and copper thickness of the impedance influence factor are zero-managed to ensure that the impedance value of the mass production is close to the median value of the theoretical design.

Module PCB Impedance Return to Zero Management:



DVCP fill plating wire,
Plted copper thick + / -3um

Copper thick

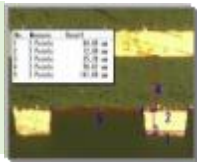
Mediate thick

line width

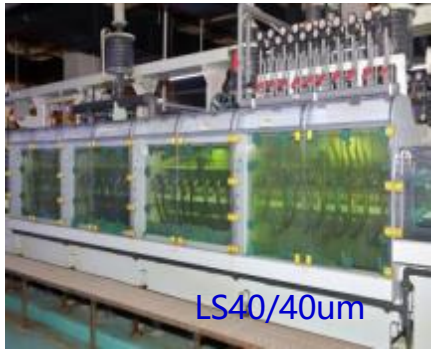
impedance

1, fully automatic AD LDI exposure machine, analysis 1.2mil ;
2. Cosmic vacuum difluid DES, uniformity> 95%;
3. Wide tolerance of internal control line + / -8%;

copper 25um、trimmings 3.8um ,
Etching factor of 7.0



1, special pressure closing program;
2. The flatness of the press is <0.15mm;
2. Automatic cutting line XRAY thickness meter, plate thickness tolerance + / -8um;



Module PCB Impedance Return to Zero Management:

Specification for the layer number of HDI plates		
condition	**Number of panels**	**remarks**
The secondary outer layer compression thickness is 0.3mm	10 layer	Middle pad twice brown paper, Use 25 pieces each New cowhide paper
Secondary outer layer 1, secondary outer layer 2 (compression thickness more than 0.3mm) P sheet (1027,1037,106)	10 layer	
First order and second order outer layer, compression thickness of 1. 0 mm P sheet (1027,1037,106)	10 layer	
Secondary outer layer 3 and above layer, press the thickness ≤1.0mm	10 layer	
Secondary outer layer 3 and above, 1.0mm <compression Thickness of 1.5mm	8 layer	
Secondary outer layer 1, secondary outer layer 2 (compression thickness more than 0.3mm)	12 layer	Middle pad of brown paper twice, Use 25 pieces of kraft paper each, 5 new + 5 * 1 times + 5 * 2 times + 5 * 3 times + 5 * 4 times =25 pieces (each Change 5 times)
First order and second order outer layer, compression thickness of 1. 0 mm	12 layer	
First and second order outer layers, 1.0mm <compression thickness ≤1.5mm	8 layer	

Module PCB impedance design recommendations:

Microstrip line impedance calculation formula:

$$Z_0 = \frac{87}{\sqrt{E_y + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

E represents the dielectric constant of the dielectric material, which is generally expressed as DK in the stacked file.
W represents the line width of the impedance line
In denotes the dielectric thickness of the alignment layer and the reference layer
t denotes the line thickness of the impedance line

It can be seen from the impedance calculation formula that the impedance value is proportional to the intermediate thickness and inversely proportional to copper thickness, wire width and Dk. At fixed frequency, Dk value is approximately a constant. In the process of PCB processing, the main factors affecting the impedance value are considered: wire width, intermediate thickness and copper thickness.

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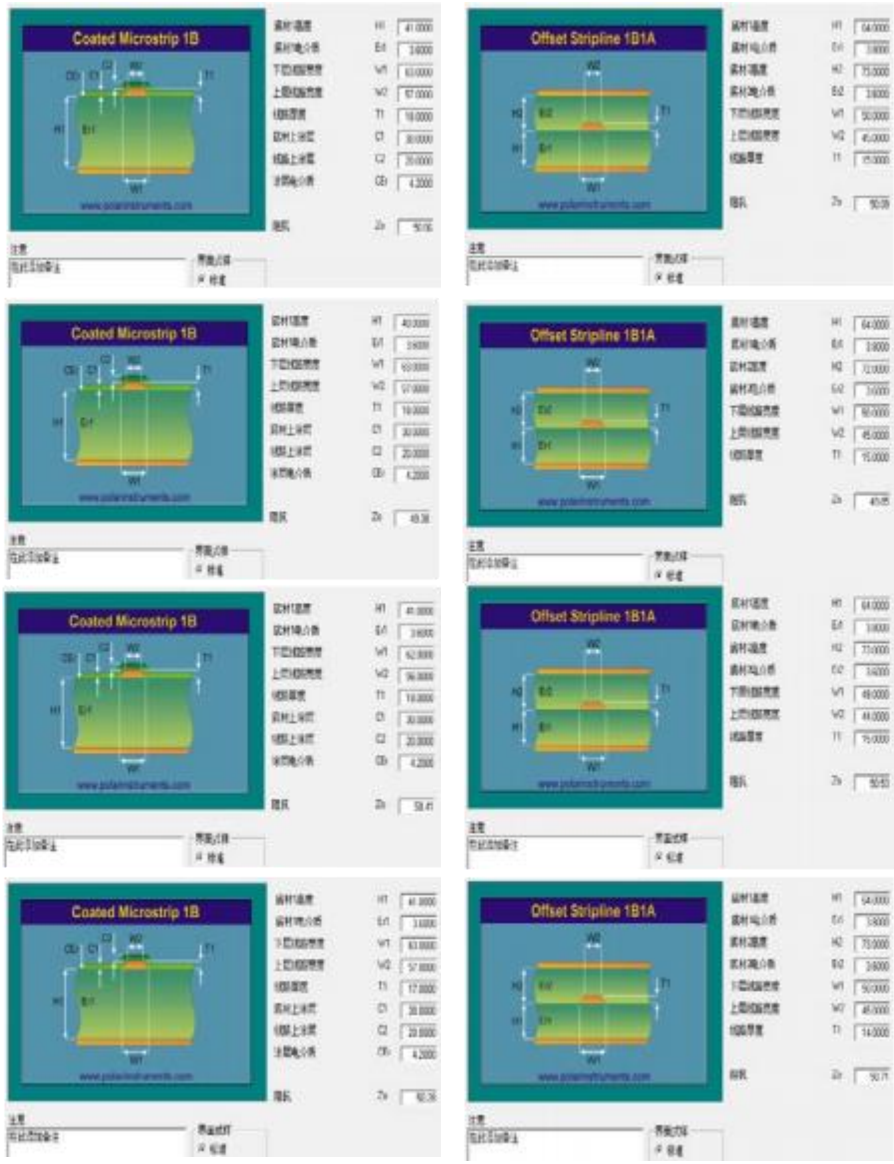
Module PCB impedance design recommendations:



project	difference	Differences in inner layer impedance	Differences in outer impedance
Mediate thick (Cu rate)	-1um	-0.25ohm	-0.68ohm
line width	-1um	+0.44ohm	+0.35ohm
Copper thick	-1um	+0.62ohm	+0.22ohm

Line width, dielectric thickness, and copper thickness, which affect the impedance value, are considered to vary by a single factor with all other factors held constant.
Under the other factors remain unchanged, a single factor change is considered:
(1) Dielectric thickness is 1um thinner, the inner layer impedance is 0.25ohm smaller, and the outer layer is 0.68ohm smaller.
0.68ohm;
(2) The line width becomes smaller by 1um, the inner layer impedance is bigger by 0.44ohm, and the outer layer is bigger by 0.35ohm.
0.35ohm;
(3) The copper thickness is reduced by 1um, the inner impedance is 0.62ohm, the outer layer is 0.22ohm.
0.22ohm;
When it is impossible to meet the impedance requirements, it is recommended to give priority to the adjustment of line width, followed by copper thickness and dielectric thickness.
thickness and dielectric thickness, it is generally recommended to adjust to:
(1) Design LS>40/40um, conventional Tenting limit, down to mSAP;
(2) Copper thickness >13um, the minimum requirement for reliability and IPC;
(3) dielectric thickness > 1027PP, dielectric thickness uniformity, filler capacity, deformation, etc.;

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Module PCB impedance design recommendations:

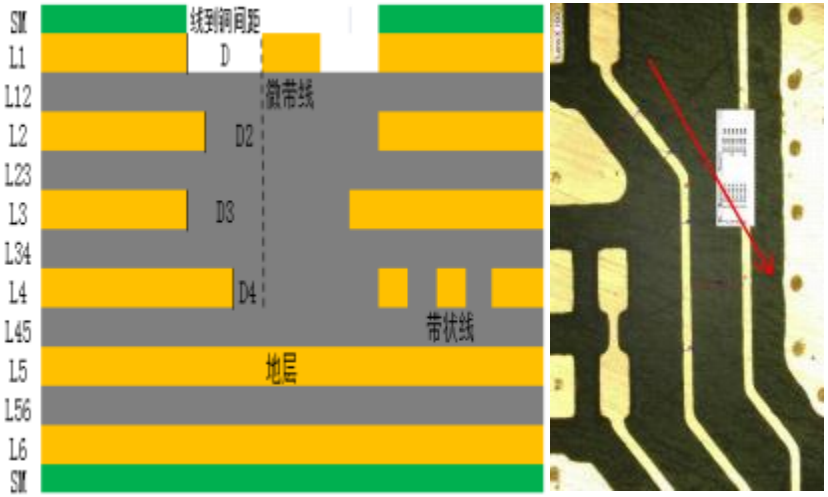
In the impedance of engineering design, due to the differences in copper residual rate and theoretical intermediate thickness, it is necessary to fine-tune the impedance line and line to copper spacing. Generally, it is recommended to follow the following principles:

1. The theoretical design impedance value is within the range of + / -1 ohm, and the impedance line adjustment shall not exceed 0.1 mil;

2. The difference of copper residual rate is within the range of 5%. Because the intermediate thickness is affected by copper thickness and compression uniformity, it is generally recommended to control + / -10% to affect the impedance 1-2 ohm;

3, the impedance generally increases with the line to copper spacing and larger, when the line to copper spacing to a certain extent, the impedance basically no longer change, the conventional impedance line to copper spacing design minimum to meet 0.5mm and more than 2 times the line width, otherwise the design, the line to copper spacing impedance calculation.

line width	Line to copper distance	impedance change	remarks
<0.175mm	> 2 Times line width	<0.5ohm	Non-coplanar impedance
	> 3 Times line width	Basically no longer change	Non-coplanar impedance
>0.175mm	> 2 Times line width	Basically no longer change	Non-coplanar impedance



Relationship between cross-plane spacing and projection distance of microstrip line:

1. When any spacing of D2 / D3 / D4 is <D, the impedance value will be less than the theoretical design impedance, and the smaller D2 / D3 / D4 is, the smaller the measured impedance value will be;

2. When D2 / D3 / D4 any spacing> D, the measured impedance value is equal to the design value, that is, when the spacing between the layer line and copper, it should be greater than the distance between the impedance signal line and copper;

3. During the impedance line design, the protective copper skin near the RF impedance line should be smooth without convex position and hole ring, so as to avoid impedance interference.

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Module PCB impedance design recommendations:

Layer	Mother Board	Tolerance (um)	Typical layer thickness (um)	Dielectric Constant	DF 1 GHz	DF 2 GHz	DF 5 GHz	DF 10 GHz
	Solder Mask	min10	15	4.2				
L1	copper+plating	25+/-10	24	NA				
	Prepreg (106)75	54+/-11	54	3.6	0.0160	0.0170	0.0190	0.0200
L2	copper+plating	20+/-10	18	NA				
	Prepreg (106)75	54+/-11	54	3.6	0.0160	0.0170	0.0190	0.0200
L3	copper+plating	20+/-10	19	NA				
	Prepreg (106)75	55+/-11	55	3.6	0.0160	0.0170	0.0190	0.0200
L4	Copper	Hoz	15	NA				
	Core	56+/-11	56	3.8	0.013	0.015	0.017	0.017
L5	copper	Hoz	15	NA				
	Prepreg (106)75	50+/-10	50	3.6	0.0160	0.0170	0.0190	0.0200
L6	Copper	Hoz	15	NA				
	Core	56+/-11	56	3.8	0.013	0.015	0.017	0.017
L7	copper	Hoz	15	NA				
	Prepreg (106)75	55+/-11	55	3.6	0.0160	0.0170	0.0190	0.0200
L8	copper+plating	20+/-10	19	NA				
	Prepreg (106)75	54+/-11	54	3.6	0.0160	0.0170	0.0190	0.0200
L9	copper+plating	20+/-10	18	NA				
	Prepreg (106)75	54+/-11	54	3.6	0.0160	0.0170	0.0190	0.0200
L10	copper+plating	25+/-10	24	NA				
	Solder Mask	min10	15	4.2				
	Total thickness	0.7+/-0.1mm	700					

Impedance	50 ohm	90 ohm	100 ohm
Reference Layer	Design L(um)	Design L/W(um)	Design L/W(um)
L1->L2	89	94 / 146	74 / 151
L1->L3	238		
L2->L1/L3	44	55 / 185	43 / 182
L3->L2/L4	43	55 / 185	43 / 182
L4->L3/L5	45	56 / 184	45 / 180
L5->L4/L6	42	53 / 187	42 / 183
L6->L5/L7	42	53 / 187	42 / 183
L7->L6/L8	45	56 / 184	45 / 180
L8->L7/L9	43	55 / 185	43 / 182
L9->L8/L10	44	55 / 185	43 / 182
L10->L8	238		
L10->L9	89	94 / 146	74 / 151

For example, 10 layers and 2 orders, ordinary Dk material is all 106PP stack, the finished plate is 0.7mm thick, which can meet the requirements of 50 / 100 impedance, without fine tuning of intermediate thickness, wire width and copper thickness.

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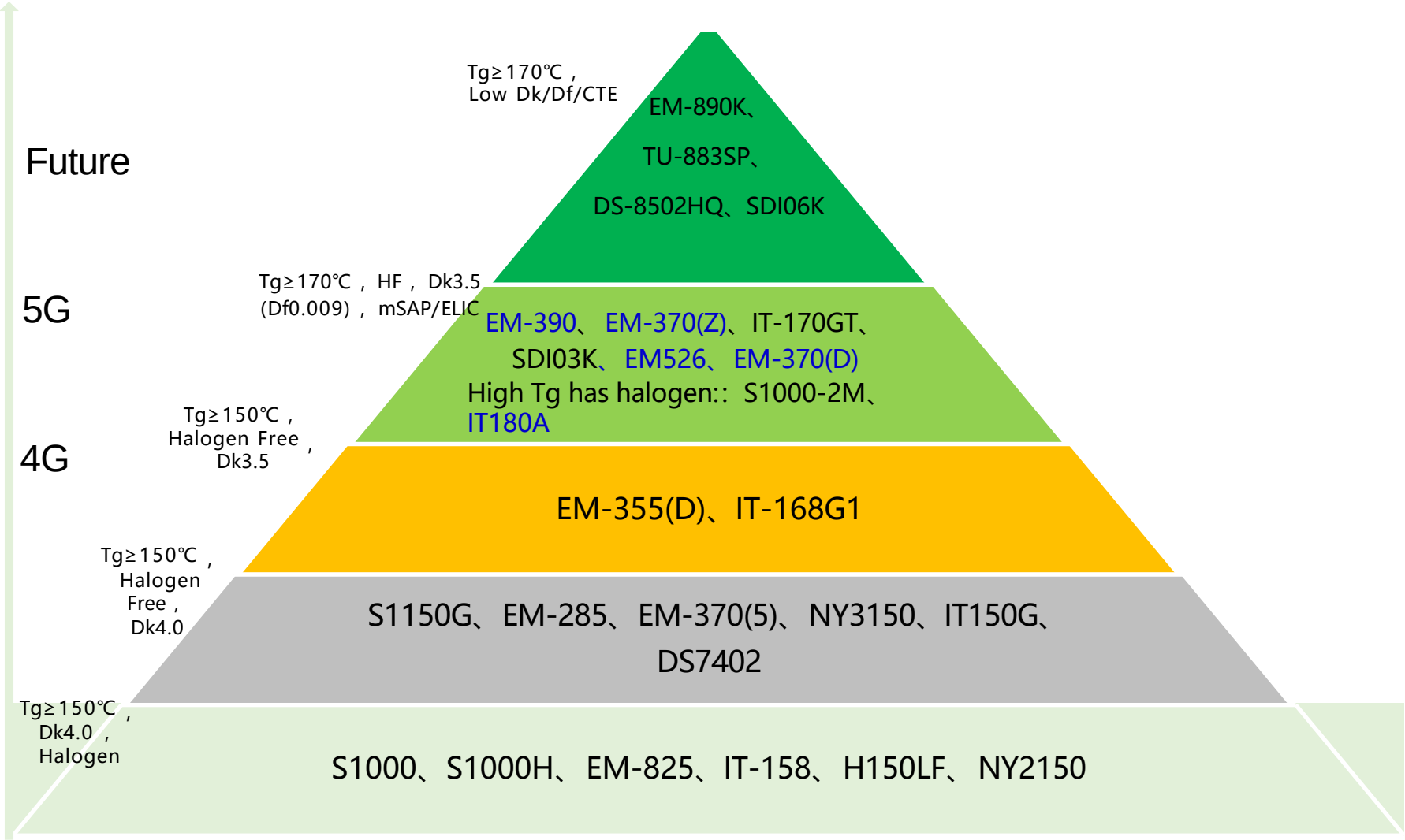
Module PCB impedance design recommendations:

Layer	Mother Board	Tolerance (um)	Typical layer thickness (um)	Dielectric Constant	DF 1 GHz	DF 2 GHz	DF 5 GHz	DF 10 GHz
	Solder Mask	min10	15	4.2				
L1	copper+plating	25+/-10	24	NA				
	Prepreg (1027)73	44+/-9	44	3.3	0.0110	0.0130	0.0140	0.0150
L2	copper+plating	20+/-10	15	NA				
	Prepreg (1027)73	43+/-9	43	3.3	0.0110	0.0130	0.0140	0.0150
L3	copper+plating	20+/-10	19	NA				
	Prepreg (1037)73	51+/-10	51	3.3	0.0110	0.0130	0.0140	0.0150
L4	Copper	Hoz	15	NA				
	Core	58+/-12	58	3.6	0.01	0.012	0.014	0.015
L5	copper	Hoz	15	NA				
	Prepreg (1037)73	45+/-9	45	3.3	0.0110	0.0130	0.0140	0.0150
L6	Copper	Hoz	15	NA				
	Core	58+/-12	58	3.6	0.01	0.012	0.014	0.015
L7	copper	Hoz	15	NA				
	Prepreg (1037)73	51+/-10	51	3.3	0.0110	0.0130	0.0140	0.0150
L8	copper+plating	20+/-10	19	NA				
	Prepreg (1027)73	43+/-9	43	3.3	0.0110	0.0130	0.0140	0.0150
L9	copper+plating	20+/-10	15	NA				
	Prepreg (1027)73	44+/-9	44	3.3	0.0110	0.0130	0.0140	0.0150
L10	copper+plating	25+/-10	24	NA				
	Solder Mask	min10	15	4.2				
	Total thickness	0.65+/-0.1mm	643					

Impedance	50 ohm	90 ohm	100 ohm
Reference Layer	Design L(um)	Design L/W(um)	Design L/W(um)
L1->L2	74	82 / 158	64 / 161
L1->L3	200		
L2->L1/L3	41(Simulated48Ohms)	48 / 192	41 / 184(Simulated97Ohms)
L3->L2/L4	41(Simulated49Ohms)	49 / 191	41 / 184(Simulated98Ohms)
L4->L3/L5	47	59 / 181	47 / 178
L5->L4/L6	44	55 / 185	44 / 181
L6->L5/L7	44	55 / 185	44 / 181
L7->L6/L8	47	59 / 181	47 / 178
L8->L7/L9	41(Simulated49Ohms)	49 / 191	41 / 184(Simulated98Ohms)
L9->L8/L10	41(Simulated48Ohms)	48 / 192	41 / 184(Simulated97Ohms)
L10->L8	200		
L10->L9	74	82 / 158	64 / 161

Module PCB material recommendation:



Conventional module products can use ordinary medium and high Tg FR4 materials, while high-end module products are generally recommended to use high Tg and Low CTE materials to reduce the module warping deformation caused by the influence of materials.

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Module PCB material recommendation:

order number	type	supplier	Material model	Material category [benchmarking material]	Tg (℃)	Td (℃)	α1(ppm/℃) [X]	α2(ppm/℃) [Y]	50-260℃(%) [Z]	water absorption rate	10Ghz	10Ghz	UL situation
12	halo gen-free	ITEQ Corporation	IT168G	FR4	153	380	40	235	3	0.12	3.8	0.009	have
13	halo gen-free	ITEQ Corporation	IT168G1	FR4	150	380	40	230	3	0.12	3.36	0.101	have
14	halo gen-free	ITEQ Corporation	IT150GS	FR4	155	365	35	230	3.1	0.12	3.9	0.012	have
15	halo gen-free	ITEQ Corporation	IT150G	FR4	150	365	35	230	3.1	0.12	3.5	0.0148	have
17	lead-free	ITEQ Corporation	IT158	FR4	155	345	40	240	3.3	0.1	4	0.018	have
21	lead-free	ITEQ Corporation	IT180A	FR4	180	350	45	210	2.7	0.1	4.1	0.016	have
54	halo gen-free	ELITE MATERIAL CO., LTD.	EM-370(D)	High-speed Mid loss 【M2】	175	385	40	180	2.2	0.13	4.00	0.015	have
55	halo gen-free	ELITE MATERIAL CO., LTD.	EM-370(Z)	High-speed Mid loss 【M2】	190	390	40	160	1.8	0.14	4.20	0.015	have
20	halo gen-free	ITEQ Corporation	IT170GT	High-speed Mid loss 【M2】	185	380	45	183	2.2	0.1	3.9	0.0095	have

order number	type	supplier	Material model	Material category [benchmarking material]	Tg (℃)	Td (℃)	Z-CTE【CTE】			water absorption rate	Dk	Df	UL situation
							α1(ppm/℃) 【X】	α2(ppm/℃) 【Y】	50-260℃(%) 【Z】		10Ghz	10Ghz	
42	halogen-free	Taiwan Sheng Yi Technology Co., Ltd.	S1150G	FR4	155	355	40	230	2.8	0.1	4.60	0.011	have
43	lead-free	Taiwan Sheng Yi Technology Co., Ltd.	S1000H	FR4	155	348	37	230	2.8	0.09	4.60	0.011	have
45	lead-free	Taiwan Sheng Yi Technology Co., Ltd.	S1000-2M	FR4	180	355	41	208	2.4	0.08	4.60	0.018	have
51	halogen-free	ELITE MATERIAL CO., LTD.	EM-285	FR4	150	360	45	220	2.8	0.11	4.20	0.011	have
52	halogen-free	ELITE MATERIAL CO., LTD.	EM-370(5)	FR4	155	385	40	200	2.6	0.13	4.30	0.013	have
53	halogen-free	ELITE MATERIAL CO., LTD.	EM-355(D)	FR4	155	385	40	220	2.8	0.1	3.40	0.013	have
56	halogen-free	ELITE MATERIAL CO., LTD.	EM-390	FR4	165(TMA)	385	40	180	2.2	0.08	3.40	0.009	have
57	lead-free	ELITE MATERIAL CO., LTD.	EM-825	FR4	150	340	45	250	3.2	0.11	4.40	0.016	have

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The Module PCB Reliability Test Plan:

order	test item	Test frequency	testing standard
1	Reflow test	100%	Refer to the customers SMT reflux furnace parameters or our own reflux furnace parameters
2	SM hardness test	1set/batch	Neither cut into nor gouge the solder mask
3	Legend/SM adhesion test	1set/batch	No obvious abnornal appearance,such as no discoloration delamination,solder mask peeling off,measling,etc.to meetIPC-A-600J Class2
4	ENIG peeling test	1set/batch	No peeling off
5	Peeling strength	1set/batch	35um copper >1.2kgf/cm2 18um copper>1.0kgf/cm2 12um copper>0.8kgf/cm2 Pad peel strength>500lb/lnch2
6	Via pull test	1set/batch	No ICD happened between the laser via battom and Target Pad.Failure mode pleases follow the attached
7	Blind hole Hot Oil Test	1set/batch	The change rate of the resistance value after the hot oil test was <10%
7	Ionic contamination test	1set/batch	≤1.56ugNaCl/cm2
8	SIR	Do the same stack structure once	Resistance>10^8Ω (after 168hrs)
9	Conductor Resistance	1set/batch	The max resistance is <=0.5ohm each 25mm(0.984inch)

The Module PCB Reliability Test Plan:

order	test item	Test frequency	testing standard
10	Insulation Resistance	1set/batch	The initial insulation ≥500Mohm After humidity testing≥100Mohm
11	Dielectric Withstanding Voltage (Hi-Pot)	1set/batch	No arc or break down
12	Solderability Test	1set/batch	The tin on the welding pad is good, and the fullness is above 95%
13	Thermal Shock Test (TST)	1set/batch	The change rate of resistance value was 10% after cold and heat shock, and there was no foaming stratification and cracking of open and blind holes
14	Hot Oil Test	1set/batch	The change rate of the resistance value after the hot oil test was <10%
15	High Current Test (HCT)	Sample stage: 100% Mass production stage: 1 pnl, 5% / batch, Anylayer100% test	No current drop, abnormal burning through
16	Thermal Stress (Solder Dip)	1set/batch	After the thermal stress test, there is no foaming layering, resistance welding ink shedding and other bad
17	Conductive Anodic Filament (CAF) Resistance	1set/batch	Post-CAF test resistance value> 100 MΩ
18	Impedance test	5set/batch	Customer processing instruction documents or EQ questions

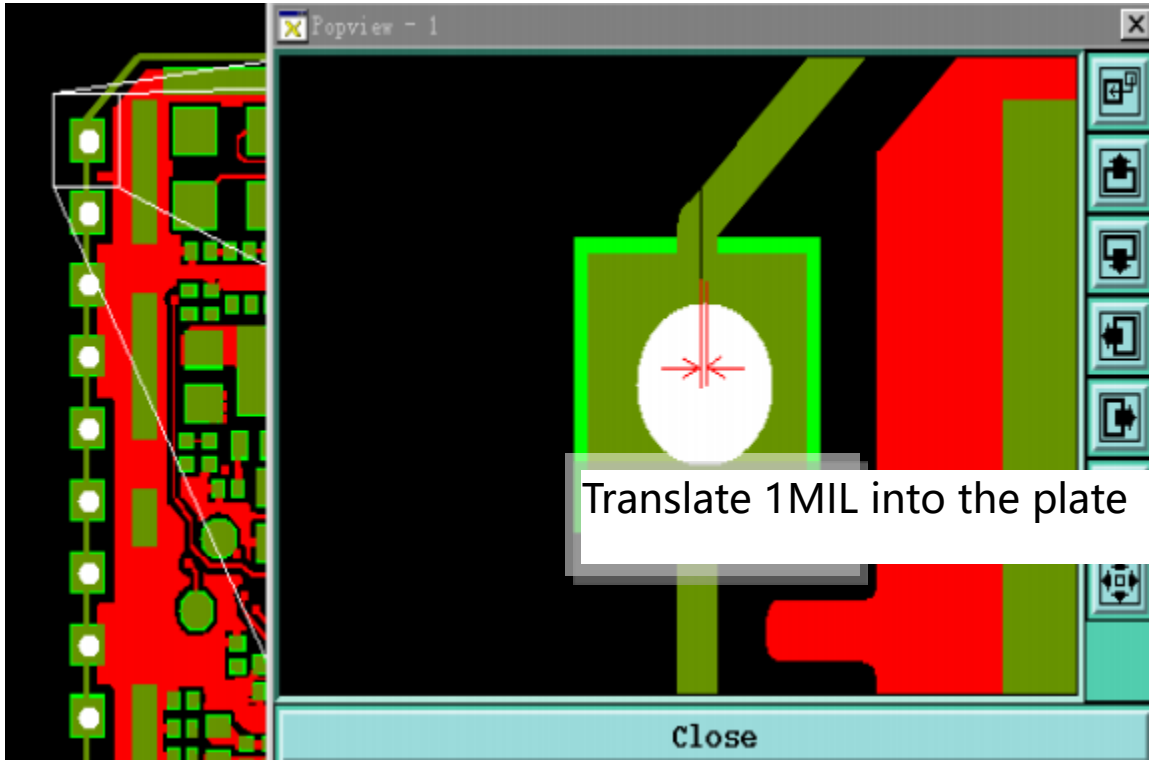
04 Module PCB Engineering Optimization advice

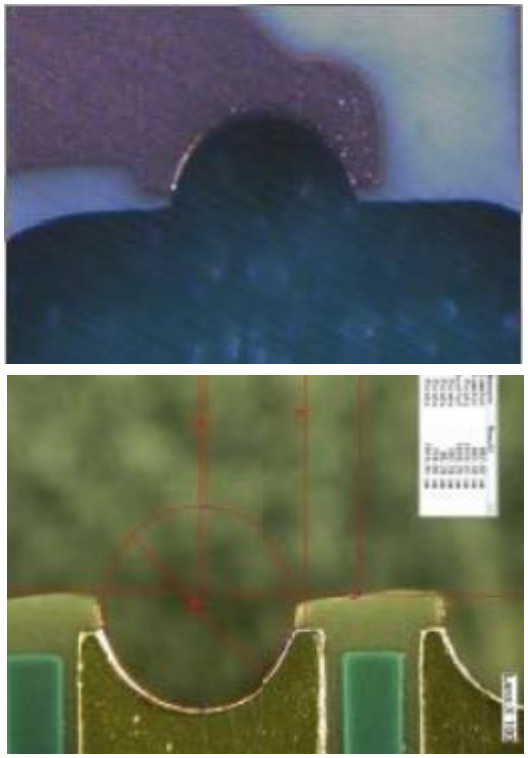
Common problems of half-hole module products: plate warping, false welding, ink into the hole:

Design Suggestions:
1) If the contact surface has a large copper surface, it is recommended not to cover the design;
2) The corresponding position of the motherboard is empty, which is convenient for the welding of half holes;
3) Increase the thickness of the tin paste in the half-hole welding position of the main board, and consider opening the step steel net;
4) Print tin paste on the auxiliary board position;
5) Cancel the text design of the contact surface;
6) If there is a space, the connection width is recommended to be above 3 mm;
7) Adopt the selective surface treatment method;

Half-hole shape circular radian:

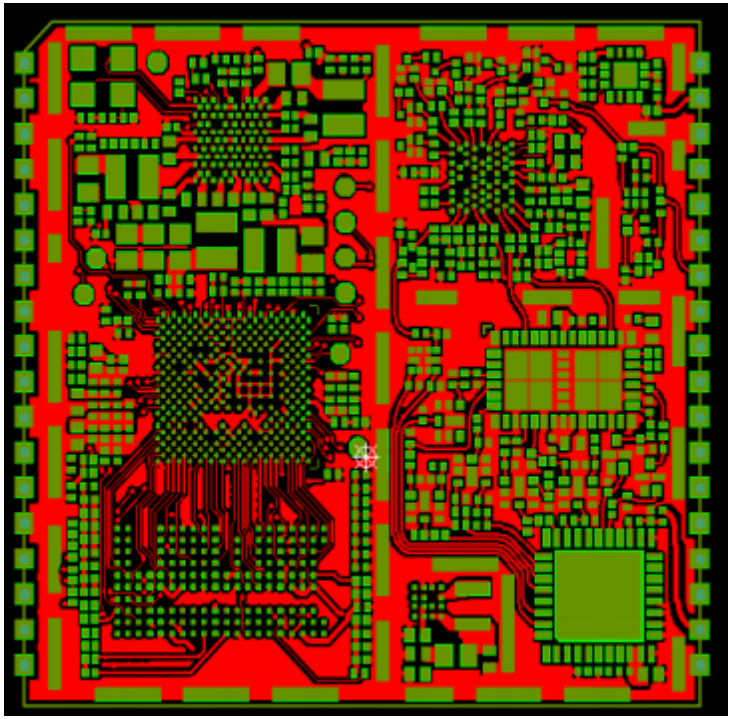
In order to ensure that the half hole arc of the finished plate is sufficient and the single shape meet the requirements, it is recommended to shift the half hole in the center of each side to the plate



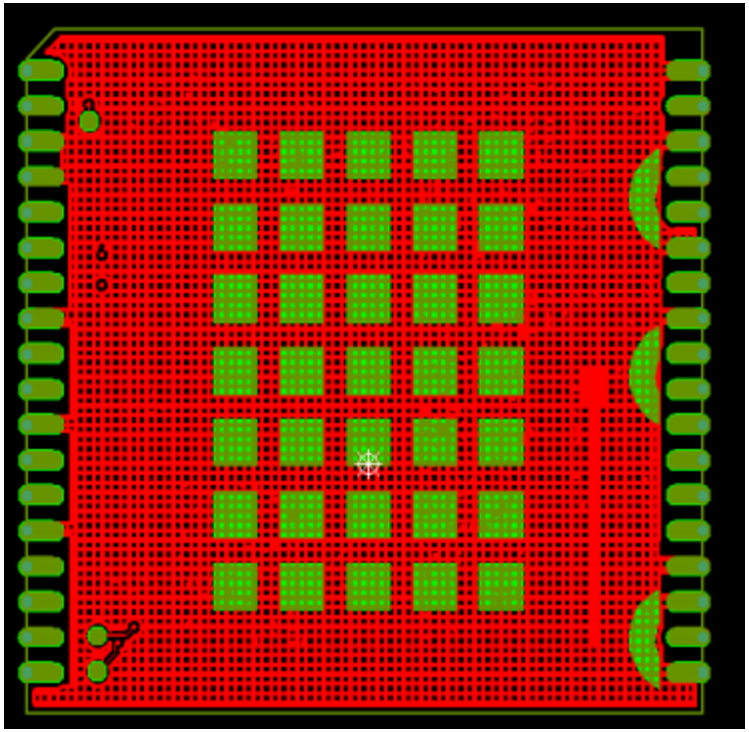


Conformity of residual copper ratio between layers:

Because the half-hole plate has strict requirements on the plate bending, in order to improve the plate warping, it is suggested that the residual copper rate of the line on both sides of the core plate should be controlled within 5%. If the residual copper rate of the symmetrical layer is greatly, the layer of copper skin with high residual copper rate is designed into a grid (the minimum mesh copper skin of our company is 10 * 10 MIL).



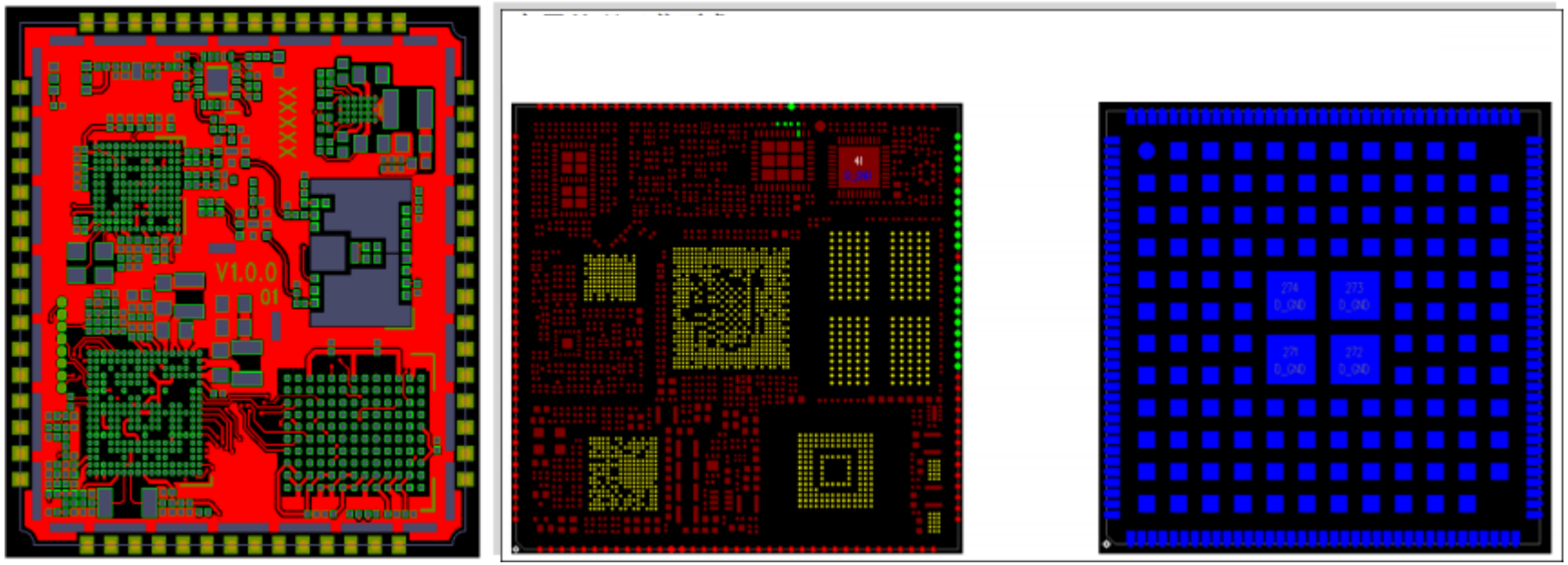
TOP layer



BOTTOM layer

surface treatment process:

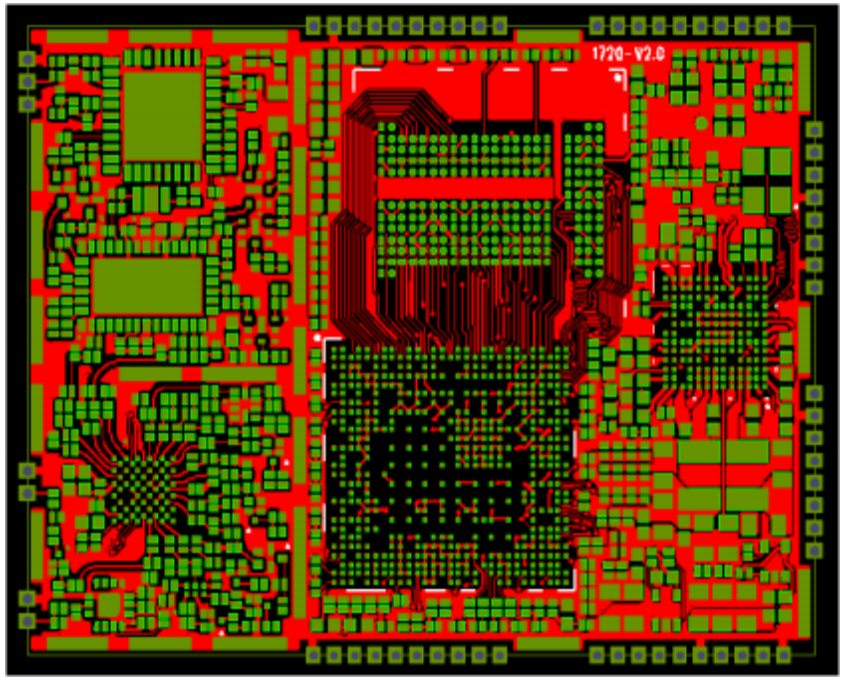
The surface treatment of the half-hole plate should be gold + OSP, with steel mesh layer, the steel mesh corresponds to the welding plate as OSP, other areas for gold, or the half-hole position as gold, and the rest should be OSP.



Surface treatment process requirements
TOP layer yellow highlight do OSP, other areas do immersion gold.
BOT layer do immersion gold on the whole surface

Combined optimization of text and weld layer:

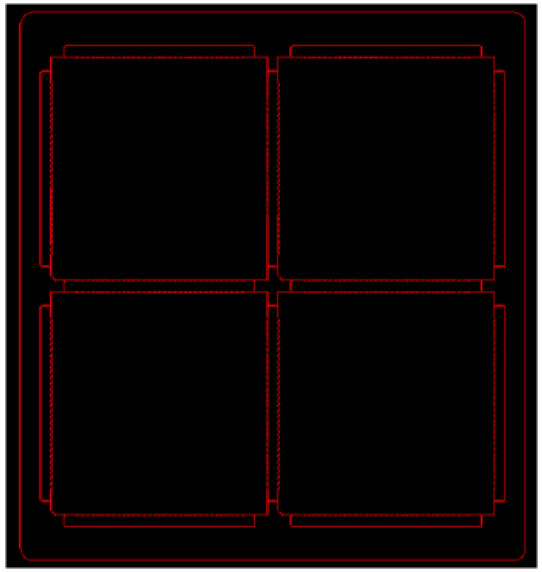
Try to design the text in the welding resistance layer, because the accuracy of the resistance welding alignment is higher than the screen printing, it is recommended to cancel the wire printing layer, the identification line and characters in the plate, are done in the welding resistance layer, in the way of resistance welding window. It can avoid the PAD on the white oil caused by the screen printing offset, improve the position accuracy of the marking line, and shorten the production time.

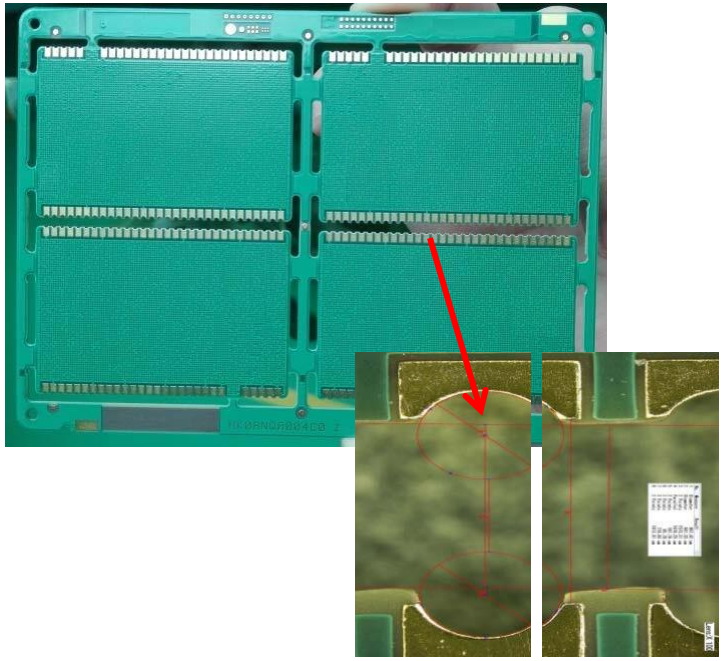


Process side design optimization:

1, for the design of products with process edge, because most of the half hole plate only four corners have a little connection position, in order to prevent the interruption in the production process, it is recommended to design according to the four side process side, and the use of physical connection, to avoid the stamp hole type weak connection;

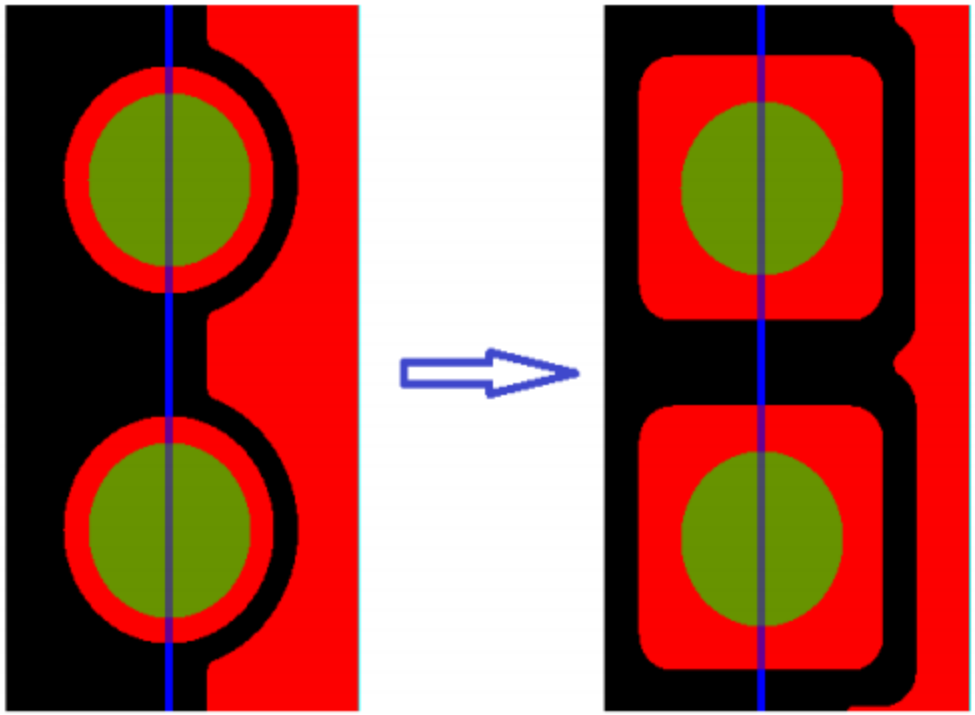
2. The commonly used gong knife is about 1.5 mm. In order to facilitate the production, it is suggested that the PCS spacing corresponding to the half-hole position should not be less than twice the diameter of the gong knife, that is, not less than 3 mm.





Design optimization of the inner half-hole ring:

The inner layer line corresponding to the half hole, the welding disc is easy to pull the hole ring into the wall in the outer hole, which affects the quality of the half hole. It is suggested to make the inner layer disc corresponding to the half hole into a square, and increase the hole ring appropriately.



Round PAD with small hole ring

Modify square PAD and add large hole ring

Copper thickness design:

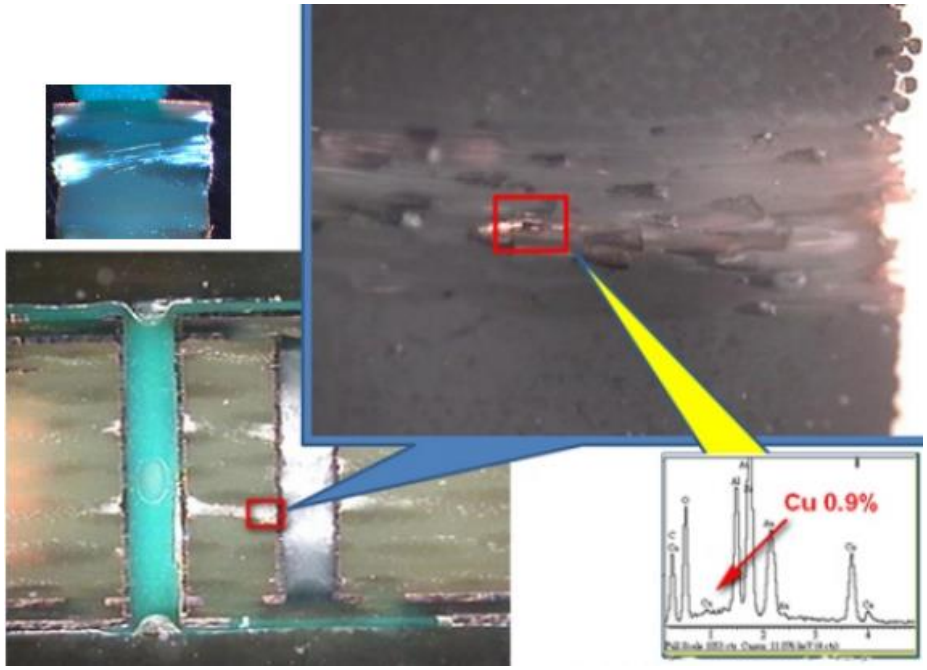
For some products, the thickness of outer hole copper is higher, such as half hole and outer hole copper 18 um (such as Z400-HEU_V3.0_Z3 project, requiring hole copper 30 um), HDI plate needs to design the hole plating process, the process becomes longer and the processing cost increases. For products with no special requirements, PTH half holes are controlled as regular Min13-15 um.

copper hole	PCB postage stamps min 18μm(standard), other min 18μm

copper hole	PCB postage stamps min 30μm(standard), other min 18μm

Wall spacing design of different network holes:

For some products, the overhole spacing of different networks is small, the buried hole design is 0.2 mm, and the minimum spacing of the hole walls of different networks is only 0.209 mm. The working draft should reduce the drilling nozzle to 0.15 mm. It is suggested that when the minimum hole is 0.20 mm, increase the distance of the hole walls between different networks to 0.275 mm to reduce the risk of CAF.



05 The module PCB case share

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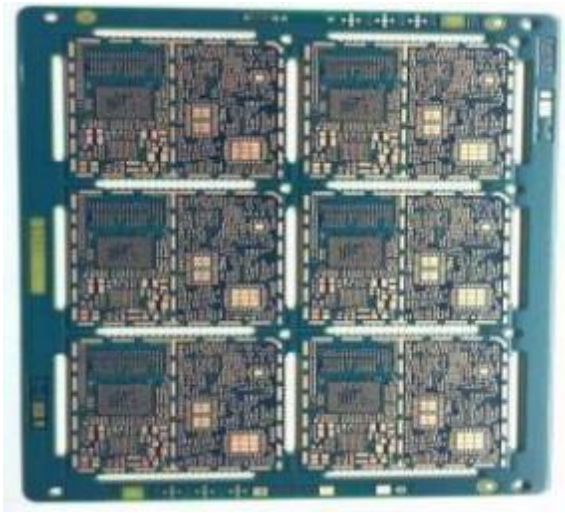
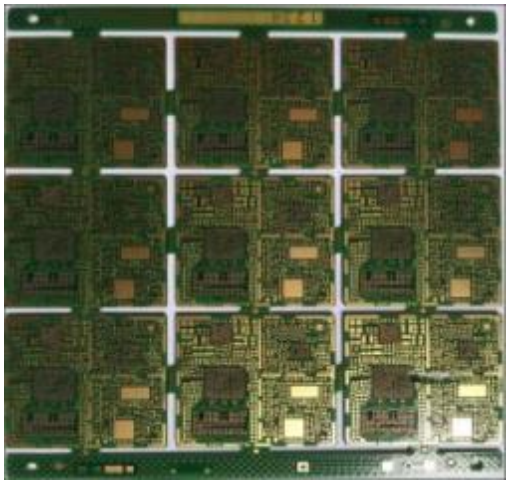
Module PCB product:



Features: The HDI half-hole module plate
Number of layers: 10 layers and order 3
Plate thickness: 0.80 + / -0.05 mm
Substrate material: FR-4
Surface treatment: gold sinking + OSP
Application field: high-end intelligent system

Features: the through-hole half-hole module plate
Number of layers: 6 layer through holes
Plate thickness: 1.0 + / -0.1 mm
Substrate material: FR-4
Surface treatment: gold sinking
Application areas: the Internet of Things



Features: The HDI half-hole module plate
Number of layers: 10 layers and order 2
Plate thickness: 1.0 + / -0.1 mm
Substrate material: FR-4
Surface treatment: gold sinking + OSP
Application areas: the Internet of Things

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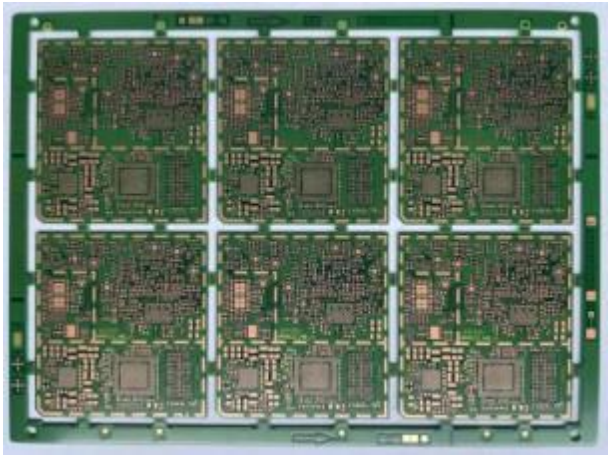
Module PCB product:



Features: The HDI half-hole module plate

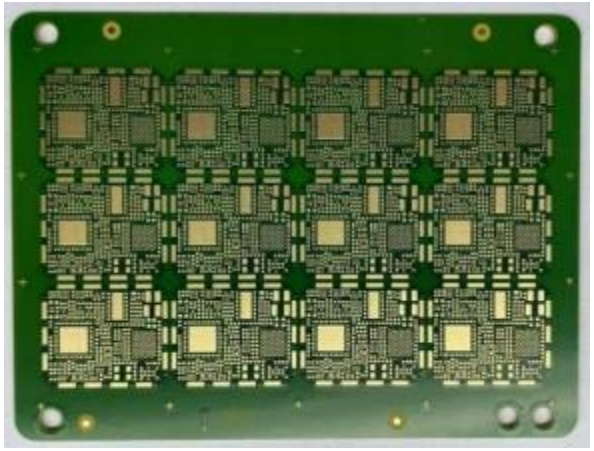
Number of layers: 10 layers and order 2

Plate thickness: 0.8 + / -0.08 mm

Substrate: EM-370 (5)

Surface treatment: gold sinking + OSP

Application areas: The Internet of Things



Features: The HDI half-hole module plate

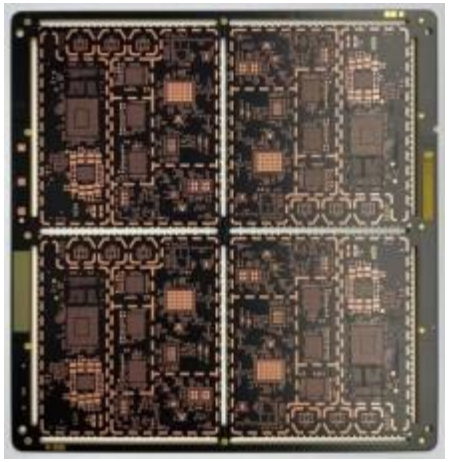
Number of layers: 8 layers and order 3

Plate thickness: 0.80 + / -0.05 mm

Substrate material: IT-170 GTTC

Surface treatment: gold sinking

Application field: communication module



Features: The HDI half-hole module plate

Number of layers: 10 layers, and the fourth order

Plate thickness: 1.2 + / -0.12 mm

Substrate material: EM-390

Surface treatment: gold sinking + OSP

Application areas: The Internet of Things

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Q&A

Thanks !